

MAHARAJA INSTITUTE OF TECHNOLOGY THANDAVAPURA

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VTU Question Papers

BE - E&C

III to VIII Semester

Jun/Jul-2023

2018 & 2021 Scheme

Maharaja Institute of Technology Thandavapura Just of NH-766,Mysore-ooty highway,Thandavapura(Vill & Post),Nanjangud Taluk,Mysore District-571302.

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18MAT31

Module-3 a. Find Fourier transform of f(x), given: 5 $f(x) = \begin{cases} 1, & |x| \le 1\\ 0, & |x| > 1 \end{cases} \text{ and hence deduce that } \int_{-\infty}^{\infty} \frac{\sin x}{x} \, dx = \frac{\pi}{2}$ (06 Marks) b. Find the Fourier cosine transform of 4x 0 < x < 1 $f(x) = \begin{cases} 4 - x & 1 < x < 4 \end{cases}$ (07 Marks) 0 x > 4 c. Solve $u_{n+2} + 4u_{n+1} + 3u_n = 3^n$, given $u_0 = 0$, $u_1 = 1$ using Z - transform. (07 Marks) OR Find the Fourier sine transform of $e^{-|x|}$ and hence evaluate $\int_{0}^{\infty} \frac{x \sin mx}{1+x^2} dx$. a. 6 (06 Marks) Find Z-transform of $\cos n\theta$ and $a^n \cos n\theta$. b. (07 Marks) Obtain the inverse Z-transform of $\frac{2z^2+3z}{(z+2)(z-4)}$. c. (07 Marks)

- a. Find the value of y at x = 0.1 and x = 0.2 given $\frac{dy}{dx} = x^2y 1$, y(0) = 1 by using Taylor's 7 series method. (06 Marks)
 - b. Compute y(0.1), given $\frac{dy}{dx} = \frac{y-x}{y+x}$, y(0) = 1 taking h = 0.1, by using Runge-Kutta 4th order method method. (07 Marks)
 - c. Find the value of y at x = 0.4, given $\frac{dy}{dx} = 2e^x y$ with initial conditions y(0) = 2, y(0.1) = 2.010, y(0.2) = 2.04, y(0.3) = 2.09 by using Milne's predictor and corrector method. (07 Marks)

a. Using modified Euler's method, find the value of y at x = 0.1, given $\frac{dy}{dx} = -xy^2$, y(0) = 2 8 taking h = 0.1. (06 Marks)

OR

- b. Solve $\frac{dy}{dx} = 3e^x + 2y$, y(0) = 0 at x = 0.1 taking h = 0.1, by using Runge-Kutta 4th order method. (07 Marks)
- c. Find the value y at x = 0.8 given $\frac{dy}{dx} = x y^2$ and 0.2 0.4 0 0 0.0200 0.0795 0.1762

By using Adam's Bashforth predictor and corrector method. (07 Marks)

18MAT31

(07 Marks)

- 9 a. Solve $\frac{d^2y}{dx^2} = x\left(\frac{dy}{dx}\right)^2 y^2$ for x = 0.2 given x = 0, y = 1 and $\frac{dy}{dx} = 0$ by using Runge-Kutta method. (07 Marks)
 - method. Derive Euler's equation in the standard form $\frac{\partial f}{\partial y} = \frac{d}{dx} \left(\frac{\partial f}{\partial y'} \right) = 0$. (06 Marks) b.
 - Find the extremal of the function $\int_{0} [(y')^2 + 12xy] dx$ with y(0) = 0 and y(1) = 1. c. (07 Marks)

OR

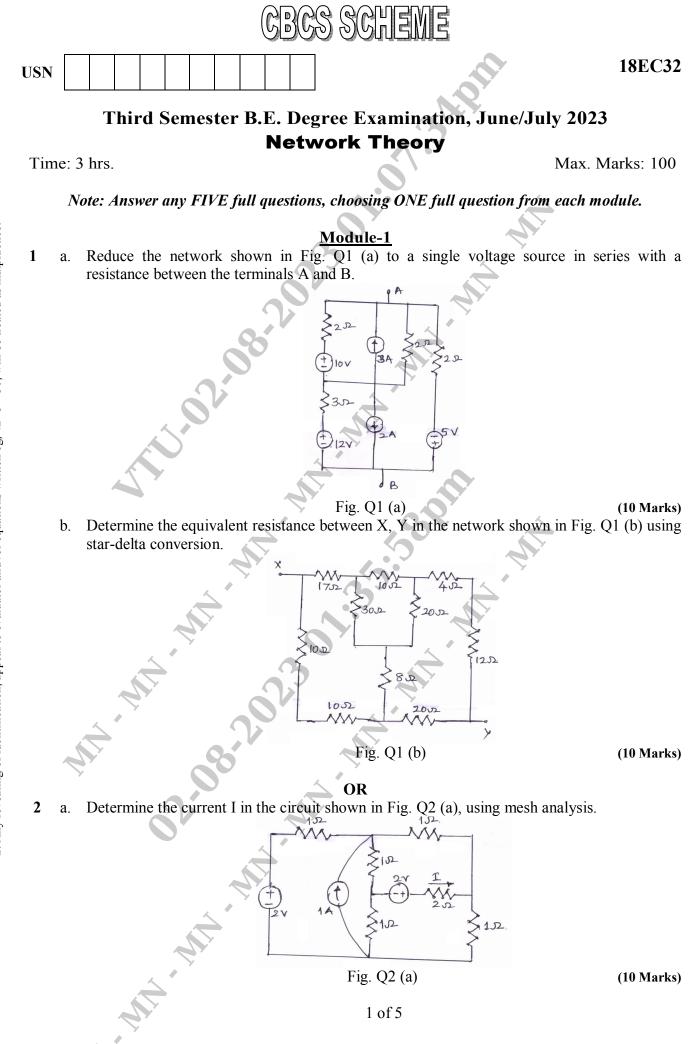
Find the value of y at x = 0.8, given $\frac{d^2y}{dx^2} = 2y\frac{dy}{dx}$ and 10 a.

ANT NATION

				dx
Х	0	0.2	0.4	0.6
у	1	0.2027	0.4228	0.6841
\mathbf{v}'	1	1.041	1.179	1.468

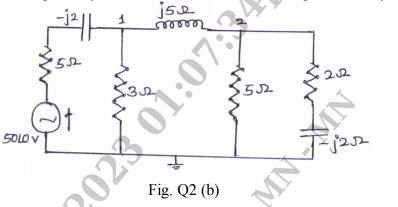
by using Milne's method.

- Prove that the shortest between two points in a plane is a straight line. b. (06 Marks)
- Find the curve on which the functional $\int [x + y + (y')^2] dx$ with y(0) = 1, y(1) = 2. (07 Marks) c.



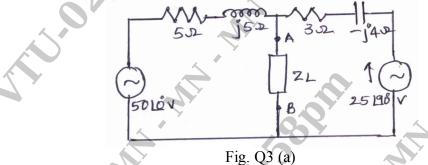
(10 Marks)

b. Determine the power supplied to the circuit shown in Fig. Q2 (b) by source $50 \ge 0^{\circ}$ V. And also find the power dissipated by each resistor in the circuit, using nodal analysis.

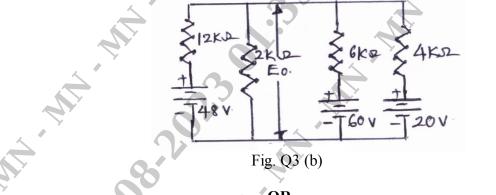


<u>Module-2</u>

3 a. In the network shown in Fig. Q3 (a), two voltage sources act on the load impedance connected to the terminals A, B. If this load is variable in both reactance and resistance, what load Z_L will receive maximum power? What is the value of the maximum power?



b. Find the output voltage E_0 for the circuit shown in Fig. Q3 (b) using Millman's theorem.



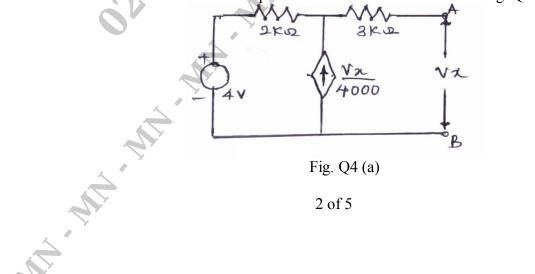
(10 Marks)

(10 Marks)

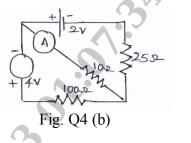
(10 Marks)

OR

4 a. Obtain Thevenin's and Norton's equivalent for the network shown in Fig. Q4 (a).



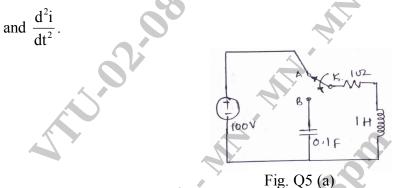
b. Determine the current through an ammeter having internal resistance of 10Ω in the network shown in Fig. Q4 (b) using superposition theorem. Verify the answer using loop current analysis.



(10 Marks)

Module-3

5 a. In the network shown in Fig. Q5 (a), steady state has been reached with the switch K on position A. The switch is moved to position B at t = 0. Determine at $t(0^+)$ the values of i, $\frac{di}{dt}$



- Fig. Q5 (a) (10 Marks) b. Explain the importance of study of initial conditions in electric circuit analysis and also explain the behavior of R, L and C elements for transients. (10 Marks)
- 6 a. In RLC series circuit shown in Fig. Q6 (a), find $i(0^+)$, $\frac{di}{dt}(0^+)$ and $\frac{d^2i}{dt^2}(0^+)$, if switch is closed at t = 0.

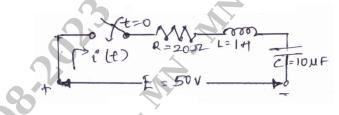
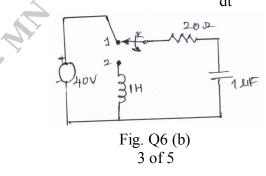


Fig. Q6 (a)

(10 Marks)

b. In the circuit shown in Fig. Q6 (b) switch K is changed from position 1 to 2 at t = 0, having been reached steady state before switching. Evaluate, i, $\frac{di}{dt}$ and $\frac{d^2i}{dt^2}$ at t = 0⁺.



(10 Marks)

Module-4

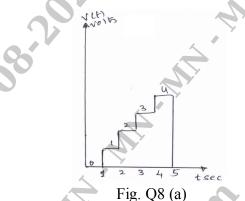
- 7 a. State and prove,
 - (i) Initial value theorem.
 - (ii) Final value theorem.
 - b. Find the Laplace transforms of following functions :
 - (i) Unit step function.
 - (ii) $f(t) = e^{at}$

(10 Marks)

(10 Marks)

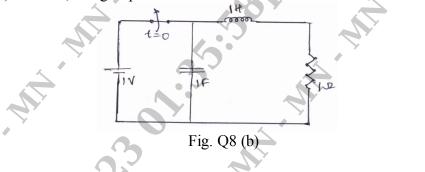
OR

8 a. Assuming that the staircase wave of Fig. $\overline{Q8}$ (a) is not repeated, find its Laplace transform. If this voltage wave is applied to a RL series circuit, with R = 1 Ω and L = 1 H, find the current i(t).



(10 Marks)

b. The network shown in Fig. Q8 (b) was in steady state before t = 0. The switch is opened at t = 0. Find i(t) for t > 0, using Laplace transform.



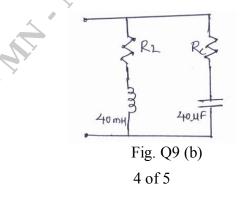
(10 Marks)

Module-5

- 9 a. Define the following terms with reference to resonance circuit:
 - (i) Resonance
 - (ii) Q-factor
 - (iii) Selectivity
 - (iv) Band width

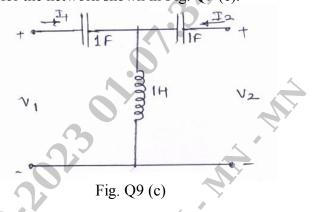
(06 Marks)

b. Determine R_L and R_C for which the circuit shown in Fig. Q9 (b) resonates at all frequencies.



(04 Marks)

c. Obtain the H-parameters for the network shown in Fig. Q9 (c).



(10 Marks)

OR

- 10 a. Obtain ABCD parameters interms of Z-parameters and hence show that AD BC = 1.
 - b. A series RLC circuit has $R = 10 \Omega$, L = 0.0 H and $C = 0.01 \mu F$ and it is connected across 10 mV supply. Calculate (i) f_0 (ii) Q_0 (iii) Bandwidth (iv) f_1 and f_2 (v) I_0 (10 Marks)



Third Semester B.E. Degree Examination, June/July 2023 Electronic Devices

Time: 3 hrs.

1

2

Max. Marks: 100

(08 Marks)

(08 Marks)

(06 Marks)

(06 Marks)

(08 Marks)

(06 Marks)

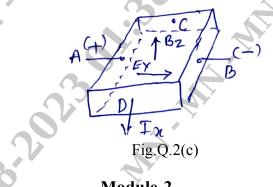
Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- a. Explain direct and indirect semiconductors with neat sketches and giving examples. (06 Marks)
- b. Define:
 - i) Intrinsic semiconductor
 - ii) Amphoteric Impurity
 - iii) Electron mobility
 - iv) Hall Effect.
- c. A silicon is doped with 10^{17} Arsenic atoms/cm³. What is the equilibrium hole concentration p_0 at 300°K? Sketch the resulting band diagram showing where is E_F relative to Ei. Assume $ni^2 = 2.25 \times 10^{20}$. (06 Marks)

OR

- a. Explain effects of temperature and doping on mobility.
 - b. Explain the formation of extrinsic semi conductor with covalent bonding model diagram. (06 Marks)
 - c. Consider a semiconductor bar with W = 0.1 mm, t = 10 mm and L = 5 mm. For $B_2 = 10 \text{kG}$ in the direction shown in Fig.Q.2(c) and a current of 1mA, $V_{AB} = -2 \text{mV}$, and $V_{CD} = 100 \text{mV}$. Find the type of semiconductor carriers and mobility of the majority carrier. Given $1\text{KG} = 10^{-5} \text{wb/cm}^2$. (06 Marks)



3 a. Differentiate Zener and Avalanche breakdown.
b. Explain the requirement for the design of rectifier diode.
c. Explain the working of solar cell and mention the applications of LED.

OR

- 4 a. Mention the applications of photo diode.
 - b. Explain the current and voltage in an illuminated junction by deriving the expression for V_{OC}. (08 Marks)
 - c. A solar cell has a short circuit current of 100mA, and an open circuited voltage of 0.8V under full solar illumination. What is the power delivered by the cell which is having a fill factor of 0.7? (06 Marks)

1 of 2

(06 Marks)

(08 Marks)

Module-3

- 5 a. Derive the relationship between α and β of a transistor.
 - b. Explain switching action of transistor.
 - A symmetrical p^+np^- bipolar transistor has the following properties: c.

	Emitter	Base
$A = 10^{-4} \text{ cm}^2$	$N_a = 10^{17}$	$N_d = 10^{15} \text{ cm}^{-3}$
$W_b = 1 \mu m$	$t_n = 0.1 \mu s$	$t_p = 10 \mu s$
	$\mu_{p} = 200$	$\mu_n = 1300 \text{cm}^2 \text{ v.s}$
	$\mu_n = 700$	$\mu_p = 450 \text{cm}^2 \text{ v.s}$
Assume $ni = 1.5$	$5 \times 10^{10} / \text{cm}^3$. F	ind base current.

(06 Marks)

OR

6	a.	Explain the working of pnp transistor with necessary figures.	(08 Marks)
	b.	Explain BJT fabrication process.	(06 Marks)
	c.	Explain drift in the base region.	(06 Marks)

Module-4

7	a.	Explain n-channel PNJFET operation with its characteristics.	(10 Marks)
	b.	Mention the difference between JFET and MOSFET.	(04 Marks)
	c.	Explain the MOS structure with aid of parallel plate capacitor.	(06 Marks)

OR

8	a.	Explain the operation of p-channel depletion	n and enhancement	type MOSFET	with neat
		sketches.			(10 Marks)
	b.	Mention the applications of MOSFET.		\leq	(04 Marks)

c. Draw and explain small signal equivalent circuit of a n-channel PNJFET. (06 Marks)

Module-5

9	a.	Mention the advantages of IC's over discrete components.	(06 Marks)
	b.	Explain photolithography process.	(06 Marks)
	c.	Explain the working of CMOS inverter with neat diagram.	(08 Marks)

OR

- Explain thermal oxidation and diffusion process of the semiconductor fabrication. 10 a.
 - (08 Marks) b. Explain integration of other circuit elements. (08 Marks) (04 Marks)
 - c. Define: i) Etching ii) Metallization.



Third Semester B.E. Degree Examination, June/July 2023 Digital System Design

Time: 3 hrs.

1

2

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- a. A switching circuit has four inputs A, B, C and D and one output F. Inputs A and B represent the bits of number N_1 , and C and D represent the bits of number N_2 . The output is to be logic 1 only if the product $N_1 \times N_2$ is lesser than 2. Obtain the minterm and maxterm expressions in decimal notation for the output F. (06 Marks)
 - b. Simplify $f(A, B, C, D) = \sum m (1, 2, 3, 5, 6, 7, 9, 10, 11)$ using K-map to get the minimum SOP expression, as well as minimum POS expression. Among the two expressions, find out which one requires lesser number of gates for implementation? (10 Marks)
 - c. Convert $X = \overline{a}b + bc$ to canonical SOP form.

OR

- a. Four chairs A, B, C and D are placed in row. Each chair may be occupied (logic 1) or not occupied (logic 0). The output Y should go high only when adjacent chairs are occupied. Draw the truth table, obtain the maxterm expression and simplify the expression using K-map to get minimum POS expression. (08 Marks)
 - b. Simplify the function $f(A, B, C, D) = \sum m(9, 12, 13, 15) + \sum d(1, 4, 5, 7, 8, 11, 14)$ using QM technique. Identify the essential prime implicant, if any, and obtain at least two solutions. (12 Marks)

Module-2

- 3 a. Give the truth table of full adder, derive the expressions for the outputs, and design a logic circuit for the same using minimum number of 2-input NAND gates only. (10 Marks)
 - b. Draw the block diagram of 4-bit look ahead carry adder. Derive the expressions for the carry outputs using propagate and generate inputs. (10 Marks)

OR

4 a. Implement full-subtractor circuit using one 3:8 decoder having active-low outputs.

(06 Marks)

(06 Marks)

(04 Marks)

- b. Implement the Boolean function $f(w, x, y, z) = \sum m(3, 5, 6, 8, 11, 13, 14, 15)$ using one 4 to 1 multiplexer and additional gates. Connect w and x inputs to select lines. (06 Marks)
- c. Explain what is FPGA? Show how a 6-varibale function can be implemented using 4-input function generators and additional hardware and implemented as FPGA. (08 Marks)

Module-3

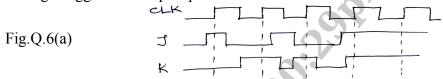
5 a. Show how an SR latch can be used for switch debouncing. Explain with waveforms.

b. Bring out the differences between gated SR latch and master-slave SR flip-flop. Draw the circuits of both. (06 Marks)

c. Draw the block diagram of 3-bit bidirectional shift register capable of serial and parallel load and explain its operation. (08 Marks)

1 of 2

6 a. Draw the Q and Q output waveforms if the waveforms given in Fig.Q.6(a) is fed to a positive edge-triggered JK flip flop. (04 Marks)



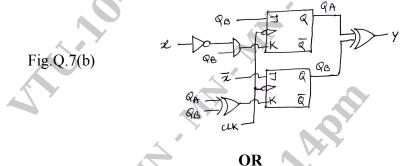
- b. Using K-map simplification, obtain the characteristic equations of SR, JK and T flip-flops, and hence construct SR, JK and T flip flops using edge-triggered D flip flop. (10 Marks)
- c. Construct a ripple counter that counts from 111 to 000 and repeats, using negative edge-triggered toggle flip-flops. Draw the waveforms showing one complete count cycle.

(06 Marks)

(12 Marks)

Module-4

- 7 a. Design a synchronous counter using JK flip flops, having the count sequence: 0, 1, 3, 5, 7 and repeats. The counter should be self-correcting if in case it goes into an unused state.
 - b. Construct the transition table, state table and state diagram for the sequential circuit shown in Fig.Q.7(b). (08 Marks)



8 a. Design a sequential circuit using JK flip flops for the state diagram shown in Fig.Q.8(a).

(12 Marks)

Fig.Q.8(a)

b. With block diagrams, explain what are Moore and Mealy models of sequential circuits. Explain with one simple each. What difference do you notice in drawing the state diagrams for both the models? (08 Marks)

oli

Module-5

- 9 a. Design a Mealy sequential circuit with one input and one output, using D flip flops, to detect the sequence 10110 with overlap. (14 Marks)
 - b. Draw the block diagram of a serial adder capable of adding two 4-bit numbers. Illustrate its working with an example. (06 Marks)

OR

- 10 a. Obtain the state diagram, state table and reduced state table for a 4-bit BCD to excess-3 sequential circuit with one input and one output. (12 Marks)
 - b. Draw the block diagram of a serial multiplier that can multiply two 4-bit unsigned numbers. Illustrate by multiplying the numbers 1011 and 1101. (08 Marks)

* * * * * 2 of 2

			CBCS	SCHEME		
USN						18EC35
		Third Semester B	0		•	
		Computer	Organiza	tion and Arcl	nitecture	
Tin	ne: 3	3 hrs.			Max. Ma	rks: 100
	N	ote: Answer any FIVE full	questions, c	hoosing ONE full qu	estion from each mo	dule.
1	0	Explain with a neat diagra		Module-1	f a Computor	(09 Marles)
1	a. b.	Explain how to measure th			n a Computer.	(08 Marks) (06 Marks)
	c.	Write a note on Types of C				(06 Marks)
			5	OR		
2	a.	Explain IEEE standard for				(08 Marks)
	b. с.	Explain the methods to im Write a note on Processor		formance of Comput	er.	(08 Marks) (04 Marks)
	U.	write a note on ribeessor	ciock.	N.		(04 Marks)
3	0	What is an Addressing Ma		<u>odule-2</u>	nodo with an oxample	
3	a.	What is an Addressing Mc		any four addressing h		(10 Marks)
	b.	With an example, explain		pt of BIG – END	AN and LITTLE –	
		Assignment of Memory St	orage.		\sim	(10 Marks)
				OR		
4	a. b.	Explain the concept of Sta What are Assembler direct			er directives with exa	(08 Marks) mples
						(08 Marks)
	C.	With an example, explain	Shift and Rot	ate Instructions.	*	(04 Marks)
		<u> </u>		odule-3		
5	a.	Define Interrupt. Explain from multiple devices.	Daisy chain a	and Priority Structure	e methods of handling	g interrupts (10 Marks)
	b.	With a neat diagram, expla	ain DMA Cor	troller Operation wit	h its Interface Registe	· · · · · ·
		\geq				(10 Marks)
				OR		
6	a.	Define Exceptions. Explai		21 1		(06 Marks)
	b. с.	Explain the Tree structure With a neat diagram, expla			arbitration schemes.	(06 Marks) (08 Marks)
			1			· · · ·
7	a.	Define Cache Memory, Ex		odule-4 types with neat diag	ram	(08 Marks)
	b.	Write a note on Classificat	tion of a Men			(04 Marks)
	C.	Define the following termsi) Memory Latency		lemory Bandwidth		
		iii) Memory Access time		lemory Cycle time.		(08 Marks)
		<u> </u>		OR		
				1 of 2		
		H. HI				
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Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. 2. Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8 = 50, will be treated as malpractice.

- 8 a. Explain with block diagram, the Operation of SD RAM. (10 Marks)
 - b. Define ROM Point out and explain various types of ROM's. (10 Marks)

Module-5

- 9 a. Explain with neat diagram, Single Bus Organisation of data path inside a processor.
 - b. What are the actions required to execute a Complete Instruction Add(R3), R1? (10 Marks) (10 Marks)

OR

- 10a. Explain Hardwired Control Unit Organisation.(10 Marks)b. Explain Multiple bus / three bus Organization, with a neat diagram.(10 Marks)
 - 2 of 2

Third Semester B.E. Degree Examination, June/July 2023 **Power Electronics and Instrumentation**

CBCS SCHEME

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- What is Power Electronic Converter System? Mention any four application of such system. a. (04 Marks)
 - b. Using two transistor model, explain the operation of SCR and derive anode current and gate relation. (08 Marks)
 - Explain different types of Power Electronic Converter Systems. Draw their Input / Output c. characteristics. (08 Marks)

OR

- Mention different Thyristor turn ON method. Mention the advantages of gate triggering. a. (04 Marks)
 - Explain the operation of Self Commutation by LC Circuit {Class B} with relevant circuit b. and waveforms. (08 Marks)
 - With a neat circuit and waveforms, explain the operation of RC Full wave firing circuit. C. (08 Marks)

Module-2

- Explain the effect of Free Wheeling Diode used in Controlled Rectifier. 3 (04 Marks) a.
 - b. With a neat circuit diagram and waveform, explain the principle operation of Step down Chopper. Derive the expression for average and r.m.s output voltage. (08 Marks)
 - c. A single phase half wave controlled rectifier has a purely resistive load of R and the delay angle is $\alpha = \pi/3$. Determine Efficiency, Form Factor, Transformer Utilization Factor and Ripple Factor. (08 Marks)

OR

- A Step up Chopper is used to deliver load voltage of 500V from a 220V d.c source. If the 4 a. blocking period of the thyristor is 80µF, compute the required pulse width. (04 Marks)
 - b. With a neat circuit diagram and wave form, explain the operation of Step Up / Down Choppers. Derive the expression for average output voltage. (08 Marks)
 - c. Explain with the help of neat circuit diagram, the operation of a single phase full converter with resistive load. Draw the associated waveform. Derive expression for r.m.s and average output voltage. (08 Marks)

Module-3

- Define Inverters. Classify the inverts according to the input source. 5 a. (04 Marks) What are Static Errors? Explain them in details. b. (08 Marks) (08 Marks)
 - Explain Multirange Ammeter and Multirange Voltmeter. C.

OR

1 of 2

USN

1

2

- 6 a. Define the terms : i) Measurement ii) Resolution iii) Precision iv) Sensitivity. (04 Marks)
 - b. Explain the Operation of Single Phase Half Bridge Inverter connected to resistive load with the help of circuit diagram and waveforms. Derive the r.m.s output voltage. (08 Marks)
 - c. Explain with a neat circuit and waveforms, the Operation of Flyback Converters. (08 Marks)

Module-4

- 7 a. The wheat stone's bridge consists of following parameters $R_1 = 10k\Omega$, $R_2 = 15k\Omega$ and $R_3 = 40k\Omega$. Find the unknown resistance R_X . (04 Marks)
 - b. With a neat block diagram, explain the working of Function Generator. (08 Marks)
 - c. Explain with a block diagram, the Operating principle of Ramp type DVM. (08 Marks)

OR

- 8 a. A Wein bridge circuit consists of the following : $R_1 = 4.7k\Omega$, $C_1 = 5nf$, $R_2 = 20k\Omega$, $C_2 = 10nf$, $R_3 = 10k\Omega$, $R_4 = 100k\Omega$. Determine the frequency of the circuit. (04 Marks)
 - b. Explain with a neat block diagram, the Operation of Successive Approximations type DVM. (08 Marks)
 - c. Explain with a neat circuit inductance comparison bridge. Also find the equivalent series circuit off the unknown impedance. An inductance comparison bridge is used to measure inductive impedance at a frequency of 5KHz. The bridge constant at balance are $L_s = 10mA$, $R_1 = 10k\Omega$, $R_2 = 40k\Omega$ and $R_3 = 10k\Omega$. (08 Marks)

Module-5

- a. Define Transducers. List the important parameters of Electrical transducer. (04 Marks)
 - b. Explain Construction and Principle Operation of LVDT. (08 Marks)
 - c. Explain the Operation of a Resistance thermometer and mention its advantages. (08 Marks)

OR

- 10 a. What are features of Instrumentation Amplifiers? How it differs from the Ordinary Op Amp? (04 Marks)
 - b. Explain with neat diagram the PLC structure.

9

c. Explain Instrumentation Amplifier using transducer bridge with the help of circuit diagram.

(08 Marks)

(08 Marks)



Fourth Semester B.E. Degree Examination, June/July 2023 Complex Analysis, Probability and Statistical Methods

Time: 3 hrs.

Max. Marks: 100

(07 Marks)

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- a. Find analytic function u + iv, where u is given to be u = e^x[(x² y²) cosy 2xy siny]. (06 Marks)
 b. Derive Cauchy Reimann equations in polar form. (07 Marks)
 c. Show that u = e^{2x} [xcos2y ysin2y] is harmonic. Find the analytic function f(z) = u + iv. (07 Marks)
 OR
 a. Derive Cauchy Reimann equation in Cartesian form. (06 Marks)
 - b. Determine analytic function f(z) = u + iv if $u v = e^x [cosy siny]$. (07 Marks) c. Show that $w = z^n$ is analytic and hence find its derivative. (07 Marks)

Module-2

- 3 a. Discuss the transformation $w = z + \frac{1}{z}, z \neq 0$. (06 Marks)
 - b. Find the Bilinear transformation which maps the points z = 1, i, -1 onto $w = 0, 1, \infty$. (07 Marks)
 - c. Evaluate $\int_{0}^{2+i} (\overline{z})^2 dz$ along i) line y = x/2 ii) real axis to 2 and then vertically to 2 + iy. (07 Marks)
 - OR
- 4 a. Discuss the transformation $w = z^2$. (06 Marks) b. State and prove Cauchy's integral formula $f(a) = \frac{1}{2} \int \frac{f(z)}{f(z)} dz$. (07 Marks)
 - c. Evaluate using Cauchy's integral formula.

|z| = 3.

$$\int_{C} \frac{e^{2z}}{(z-1)(z-2)} dz$$

Module-3

- **5** a. Define: i) Random variable ii) Discrete probability distribution with an example.
 - (06 Marks) b. The probability that man aged 60 will live upto 70 is 0.65. What is the probability that out of 10 men, now aged 60 i) Exactly 9 ii) atmost 9 iii) Atleast 7 will live up to age of 70 vears. (07 Marks)
 - c. In a normal distribution, 3% of items are under 45 and 8% are over 64. Find the mean and standard deviation, given that A(0.5) = 0.19 and A(1.4) = 0.42. (07 Marks)

OR

6 a. The probability distribution of a finite random variable X is given by

X :	-2	-1	0	1	2	3	
P(x) :	0.1	Κ	0.2	2K	0.3	Κ	

Find 'K', mean and variance of X.

Fit the curve of the

8

9

a.

a.

b.

- b. If probability of bad reaction from certain injection is 0.001. Determine the chance that out of 2000 individuals more than two will get bad reaction, and less than two will get bad reaction.
 (07 Marks)
- c. The frequency of accidents per shift in a factory is shown in the following table:

Accidents per shift	0	1	2	3	4	\leq
Frequency	192	100	24	3	1	Y

Calculate mean numbers of accidents per shift. Find the corresponding Poisson distribution. (07 Marks)

Module-4

7 a. Fit a second degree parabola $y = a + bx + cx^2$ for the following data:

Х	0	1	2	3	4	5		
у	1	3	7	3	21	31		

(06 Marks)

(07 Marks)

b. Find the coefficient of correlation, lines of regression of x on y and y on x. Given,

х	1	2	3	4	5	6	7
у	9	8	10	12	11	13	14

c. If θ is an acute angle between line of regression, then show that $\tan \theta = \frac{\sigma x}{\sigma_x^2 + \sigma_y^2} \left(\frac{1-r}{r}\right)$. Indicate the significance of the cases r = 0 and $r = \pm 1$. (07 Marks)

	OR OR											
e fo	rm	ax ^b and	d hence	e estim	ate y v	when x	= 8.					
,	X	5	10	15	20	25	30	35				
\leq	v	2 76	3 1 7	3 44	3 64	3 81	3.95	4 07				

(06 Marks)

Find the rank correlation coefficient for the following data: 44 53 08 93 71 81 10 32 31 Х 6 45 62 12 28 92 84 73 3 51 32

(07 Marks)

c. With the usual notations compute \overline{x} , \overline{y} and r from the following lines of regression: y = 0.516x + 33.73 and x = 0.512y + 32.52. (07 Marks)

	111	Juui	C- 3							
The joint probability distribution for following data										
	X Y	-2	-1	4	5					
	1	0.1	0.2	0	0.3					
	2	0.2	0.1	0.1	0					

Determine the marginal distributions of X and Y also calculate E(x), E(y), COV (xy). (06 Marks)

b. Define: i) Null hypothesis ii) Confidence limits iii) Type I, Type II errors. (07 Marks)

(06 Marks)

c. The following table gives the distribution of digits in the numbers chosen at random from a telephone directory:

Digits	0	1	2	3	4	5	6	7	8	9
Frequency	1026	1107	997	966	1075	933	1107	972	964	853

Test whether the digits may be taken to occur equally frequently in the directory.

OR

(given $\chi^2_{0.05} = 16.92$ at n = 9).

- 10 a. A fair coin is tossed thrice. The random variable X and Y are defined as follows. X = 0 or 1 according as head or tail occurs on first loss, Y = number of heads.
 - i) Determine distribution of X and Y.
 - ii) Joint probability distribution of X and Y.
 - iii) Expectation of X, Y and XY.
 - b. It is claimed that a random sample of 49 tyres has a mean life of 15200km. Is the sample drawn from population whose mean is 15,150km and standard deviation is 200km? Test the significance level at 0.05 level. (07 Marks)
 - c. Ten individuals are choosen at random from the population and their height in inches are found to be 63, 63, 66, 67, 68, 69, 70, 70, 71, 71. Test the hypothesis that the mean height of universe is 66' (value of $t_{0.05} = 2.262$ for 9.D.F). (07 Marks)



(06 Marks)

(07 Marks)

USN

18EC42

Fourth Semester B.E. Degree Examination, June/July 2023 **Analog Circuits**

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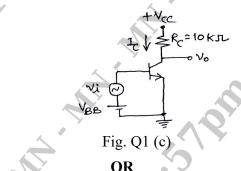
Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- What is meant by biasing of a transistor? Explain the classical bias arrangement for BJT and 1 a. derive the expressions for collector current and collector-emitter voltage. (08 Marks)
 - b. Design a collector-base feedback bias circuit to obtain $I_E = 1$ mA and $V_{CE} = 2.3$ V, assuming $V_{CC} = 10 \text{ V}, \ \beta = 100 \text{ and } V_{BE} = 0.7 \text{ V}.$ (06 Marks)
 - c. For the conceptual amplifier circuit shown in Fig. Q1 (c), draw the hybrid π model. Suppose if $I_C = 1$ mA, $\beta = 100$ and $V_T = 26$ mV, calculate the input resistance at the base and voltage gain.



(06 Marks)

OR

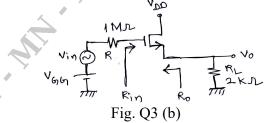
- In the classical MOSFET bias arrangement, explain how the source resistor provides 2 negative feedback action. How does this stabilize the variations in the bias current?
 - (04 Marks) b. Design a voltage divider biasing arrangement to establish a drain current of 2 mA. The MOSFET has $V_t = 1 V$, $K'_n W/L = 1 mA/V^2$. Assume $V_{DD} = 12 V$, $V_{DS} = 5 V$ and $V_S = 2 V$. (10 Marks)
 - Starting from the conceptual MOSFET amplifier circuit, draw the small-signal model of MOSFET with $\lambda \neq 0$ and derive the expressions for g_m and A_V . (06 Marks)

Module-2

With a neat circuit diagram and ac equivalent circuit, derive the expressions for Rin, Ro, Avo and A_V in a common-source MOSFET amplifier with un-bypassed source resistor.

(07 Marks)

b. For the common drain circuit shown in Fig. Q3 (b), if $I_D = 8$ mA, $V_{0V} = 1$ V and $\lambda = 0$, determine the values of R_{in}, R₀, A_{VO} and A_V. Draw the ac equivalent circuit.



(07 Marks)

c. For n-channel MOSFET with $t_{OX} = 10$ nm, $W = 10 \ \mu m$, $L = 1 \ \mu m$, $L_{OV} = 0.05 \ \pi m$, $C_{Sbo} = C_{dbo} = 10$ fF, $V_O = 0.6$ V, $V_{SB} = 1$ V and $V_{DS} = 2$ V, calculate C_{OX} , C_{OV} , C_{gs} , C_{gd} , C_{sb} and C_{db} in saturation region. Assume $\epsilon_{\rm OX}=3.45{\times}10^{-11}$ F/m. (06 Marks)

3

- 4 a. Draw and explain the high frequency response of a common-source amplifier. Derive the expression for its upper cut off frequency. (10 Marks)
 - b. Design an RC phase-shift oscillator using MOSFET having $g_m = 5000 \ \mu\text{S}$, $r_d = 40 \ \text{K}\Omega$ and feedback circuit resistor $R = 10 \ \text{K}\Omega$. Select the value of capacitor to get 1 kHz oscillations. Find R_D to get a gain of 40. (06 Marks)
 - c. Explain the series and parallel resonance actions with equivalent circuits and expressions of a crystal oscillator. (04 Marks)

Module-3

5

- a. Draw the four basic negative feedback topologies and explain each in brief. (12 Marks)
 b. Determine the voltage gain, input resistance and output resistance with feedback for a voltage series feedback amplifier having A = 10,000, R_i = 10 KΩ and R_o = 20 KΩ if β = 0.5. (04 Marks)
 - By deriving the relevant expressions, prove that negative feedback de-sensitizes the gain and increases the bandwidth. (04 Marks)
- 6 a. What is the function of output stage? Discuss the classification of output stage based on the collector current. (10 Marks)

OR

- b. A transformer coupled class-A amplifier draws a current of 200 mA from the collector supply voltage of 10 V, when the signal is not applied. If the load across the secondary is 10 Ω and the turns ratio is 5 : 1, determine (i) max output power (ii) max collector efficiency. (04 Marks)
- c. Explain the class-B output stage. Prove that the maximum conversion efficiency of class-B transformer coupled amplifier is 78.5%. (06 Marks)

Module-4

- 7 a. With circuit diagram and waveform, explain the inverting amplifier using op-amp. Derive the expressions for the exact and ideal closed-loop voltage gains. (08 Marks)
 - b. An op-amp having $A = 2 \times 10^5$, $R_i = 2 M\Omega$, $R_O = 75 \Omega$, $f_O = 5$ Hz is connected as noninverting amplifier with $R_f = 47 K\Omega$ and $R_1 = 2.2 K\Omega$. Compute the values of A_f , R_{if} , R_{of} and f_F . (08 Marks)
 - c. Give two reasons why an open loop op-amp is not suitable for linear applications. How is this overcome by using negative feedback? (04 Marks)

OR

- 8 a. With circuit diagram, explain the working of inverting scaling amplifier, averaging circuit and summing amplifier. Derive the expressions for output voltage. (07 Marks)
 - b. Explain the operation of instrumentation amplifier using transducer bridge, with diagram and relevant expressions. (08 Marks)
 - c. Draw and explain the basic non-inverting comparator circuit with waveform. (05 Marks)

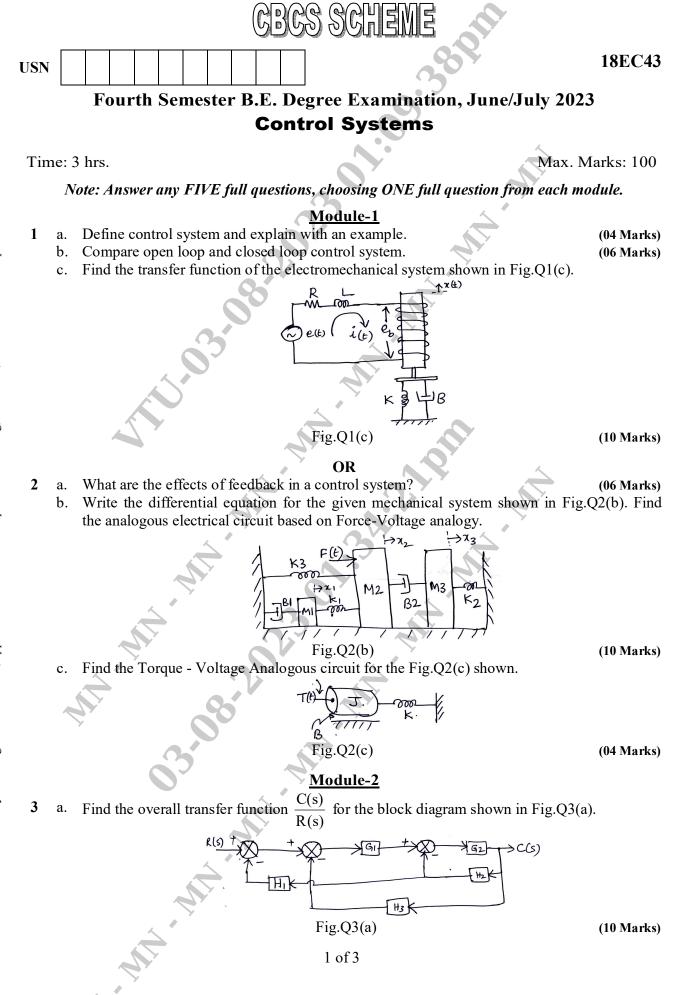
Module-5

- 9 a. Explain the working of R-2R DAC with circuit diagram, graph and expressions. (06 Marks)
 - b. For a 4-bit binary weighted resistor DAC with $R = 10 \text{ K}\Omega$, $R_f = 1.2 \text{ K}\Omega$ and $V_R = 5 \text{ V}$, determine the step size and full scale output voltage. (04 Marks)
 - c. With circuit diagram and waveform, explain the working of small-signal half wave rectifier using (i) one diode, (ii) two diodes. What is the use of the second diode? (10 Marks)

OR

- 10 a. Define the terms pass-band, stop-band, cut-off frequency and gain roll-off rate with references to the filters. What is the relation between the order and gain roll-off rate?
 - b. Design a second order Butterworth high-pass filter to have a cut-off frequency of 1.2 kHz, choosing $C_1 = C_2 = 4.7$ nF. Draw the circuit and plot the frequency response. (10 Marks)
 - c. An astable multivibrator circuit using 555 timer has $R_A = 2.2 \text{ K}\Omega$, $R_B = 3.9 \text{ K}\Omega$ and $C = 0.1 \mu\text{F}$. Determine the frequency and duty cycle of the output waveform. Draw the circuit diagram. (05 Marks)

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b. Find the transfer function by constructing a block diagram for the circuit shown in Fig.Q3(b)

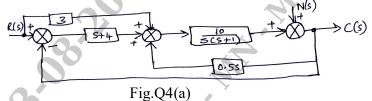
$$E_{x}(t) \bigoplus_{i_{1}(t)}^{\mathbf{K}_{1}} \bigvee_{i_{1}(t)}^{\mathbf{V}_{1}} \bigcup_{i_{2}(t)}^{\mathbf{C}_{2}} \overline{T}$$

$$Fig.Q3(b)$$
OR

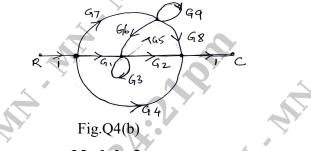
(10 Marks)

(10 Marks)

4 a. Find $\frac{C(s)}{R(s)}$ when N(s) = 0 for the diagram shown in Fig.Q4(a).



b. Find $\frac{C}{R}$ using Mason's Gain formula for the signal flow graph shown in Fig.Q4(b).



(10 Marks)

<u>Module-3</u>

5 a. A unity feedback system is characterized by an open loop transfer function

$$G(s) = \frac{K}{s(s+10)}$$

Find the value of K so that the system will have a damping ratio of 0.6, for this value of K find M_p , T_p and T_s for a unit step input. (08 Marks)

b. Find the error constants k_p, k_v and k_a for the unity feedback control system whose open loop transfer function

$$G(s) = \frac{100}{s^2(s+2)(s+5)}$$

Find the steady state error when the input $r(t) = 1 + t + 2t^2$. What is the type and order of the system? (08 Marks)

c. With the neat diagram write a note on PID controller. (04 Marks)

OR

- 6 a. Starting from output equation C(t), derive the expression for peak time, peak overshoot, settling time of an under damped second order system subjected to unit step input. (10 Marks)
 - b. Obtain rise time, peak time, % peak overshoot, settling time for the unit step response of a closed loop system given by

$$\frac{C(s)}{R(s)} = \frac{25}{s^2 + 6s + 25}$$

Also find the expression for the output.

(10 Marks)

<u>Module-4</u>

- 7 a. For a unity feedback system whose open loop transfer function is $G(s) = \frac{k(s+4)}{s(s+1)(s+2)}$ Find the range of k that keeps the system stable using R-H criteria. (08 Marks)
 - b. Sketch the Root Locus diagram for the unity feedback control system with

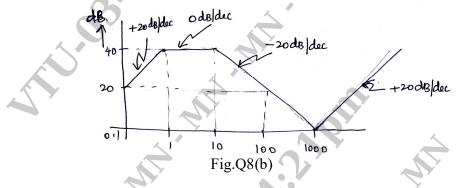
$$G(s) = \frac{k}{s(s^2 + 8s + 17)}$$
. Determine the value of k for a damping ratio of 0.5. (12 Marks)

> OR

8 a. For a system having open loop transfer function given by $G(s) = \frac{10(1+0.125s)}{s(1+0.5s)(1+0.25s)}$

Draw the Bode magnitude and phase plot. Determine the Phase margin and Gain margin. Comment on the stability. (10 Marks)

b. Find the transfer function of the system whose Bode diagram is shown in Fig.Q8(b).



<u>Module-5</u>

9 a. The open loop transfer function of a unity negative feedback control system is given by k(s+3)

$$G(s) = \frac{K(s+3)}{s(s^2+2s+2)}$$

using Nyquist criteria find the value of k for which the closed loop system is stable.

- b. Explain lead-lag compensating network. (10 Marks) (04 Marks)
- c. Represent the differential equation given below in state model

$$\frac{d^{3} y(t)}{dt^{3}} + 3\frac{d^{2} y(t)}{dt^{2}} + 6\frac{d}{dt}\frac{y(t)}{t} + 7y(t) = 2u(t)$$
(06 Marks)
OR

10 a. Mention the properties of State Transition Matrix.

b. Obtain the state model of the given network shown in Fig.Q10(b) in standard form.

(08 Marks)

(04 Marks)

(10 Marks)

c. Find the state transition matrix for the state equation given below.

$$\begin{bmatrix} \dot{\mathbf{x}}_1 \\ \dot{\mathbf{x}}_2 \end{bmatrix} = \begin{bmatrix} \mathbf{1} & \mathbf{0} \\ \mathbf{1} & \mathbf{1} \end{bmatrix} \begin{bmatrix} \mathbf{x}_1 \\ \mathbf{x}_2 \end{bmatrix} + \begin{bmatrix} \mathbf{1} \\ \mathbf{1} \end{bmatrix} \mathbf{u}(\mathbf{t})$$
(08 Marks)

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Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. 2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

and "0" For a bivariate random variable CDF is given by $c(x+1)^2$ $(y+1)^2$ for b.

outside. Find:

- The value of 'c' i)
- ii) **Bivariate PDF**
- $F_x(x)$ and $F_y(y)$ iii)
- Evaluate $P\{(x \le 2) \cap (y \le 1)\}$ iv)
- Are there variables independent? v)
- Explain briefly the following random variables: c.
 - Chi-square random variable i)
 - ii) Student-t random variable.

Module-3

- Define random process, with help of examples discuss different types of random processes. 5 a. (08 Marks)
 - Explain strict-sense-stationary and wide-sense-stationary random process. (04 Marks) b.
 - c. A random process is defined by $x(t) = A \sin(w_c t + \Theta)$ where A, w_c are constants and Θ is a uniformly distributed random variable, distributed between $-\pi$ and π . Check whether x(t) is WSS. If yes list its mean and ACF. (08 Marks)

OR

- 6 Define Auto Correlation Function (ACF) of a random process and discuss its properties. a.
 - (10 Marks) The random process x(t) and y(t) are jointly wide-sense stationary and independent. Given b. that W(t) = x(t) + y(t) and

 $R_x(\tau) = 10e$

$$R_{y}(\tau) = 10^{\left\lfloor \frac{\tau-\tau}{3} \right\rfloor} - 3 \le \tau \le 3$$
$$= 0 \text{ (otherwise)}$$

For W(t), find i) ACF ii) Total power iii) ac power iv) dc power v) check whether W(t) is W.S.S.(10 Marks)

Module-

7	a. Define vector space and explain four fundamental subspaces with example.	(08 Marks)
	b. Determine the column space and null space of the matrix $B = \begin{bmatrix} 0 & 0 & 3 \\ 1 & 2 & 3 \end{bmatrix}$.	(06 Marks)

to the Echelon (u) form and find the rank of the matrix. Reduce the matrix A c.

(06 Marks)

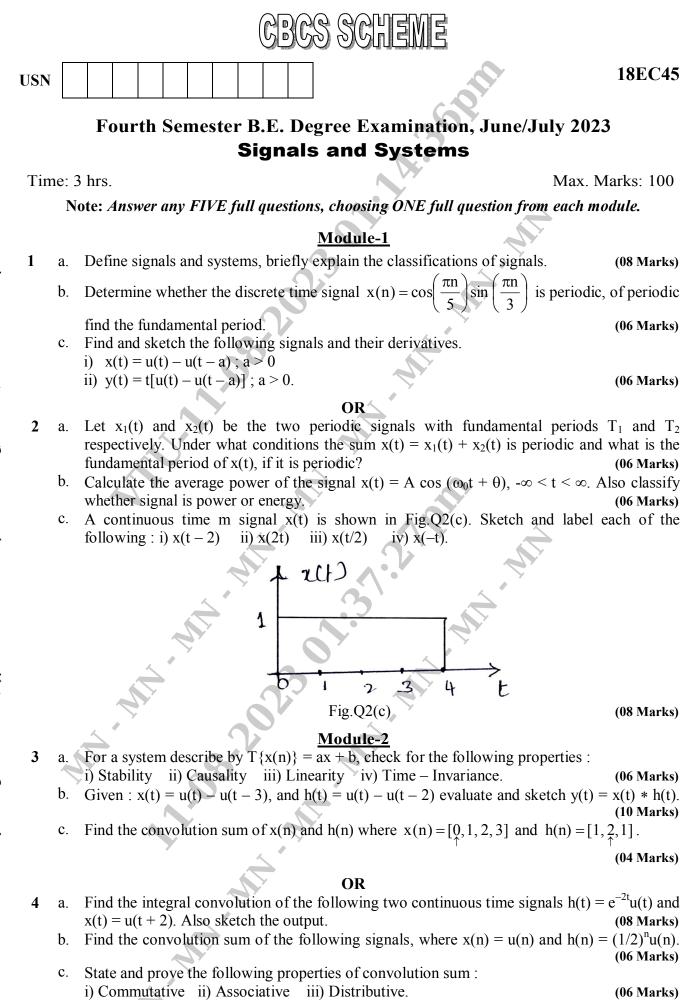
OR

What is basis for a vector space? Explain. 8 a. (06 Marks) Given the vectors (1, -3, 2), (2, 1, -3) and (-3, 2, 1). Identify the basis. Verify they are b. independent or not. (08 Marks)

(10 Marks)

(04 Marks)

18EC44 Determine orthonormal vectors for u =2 and v =(06 Marks) c. -1 Module-5 9 a. By applying row operations to produce upper triangular matrix u, compute |A| (det A). $2^{\overline{}}$ 1 5 2 6 2 3 7 1 A = (08 Marks) 2 3 1 iii) $|\mathbf{u}^{-1}|$ b. For the given upper triangular matrix, determine i) |u|ii) u 2 8 2 2 u = (06 Marks) 0 2 6 What is cofactor? Explain with an example. C. (06 Marks) OR 10 a. Find x, y and z using CRAMER's rule for the system of equations, x + 4y - z = 1x + y + z = 0 $2\mathbf{x} + 3\mathbf{z} = \mathbf{0}.$ (06 Marks) Determine the eigen values of matrix A =b. (04 Marks) i) List the properties of Singular Value Decomposition (SVD). c. ii) Prove that Identity matrix is positive definite using all required tests. (10 Marks)

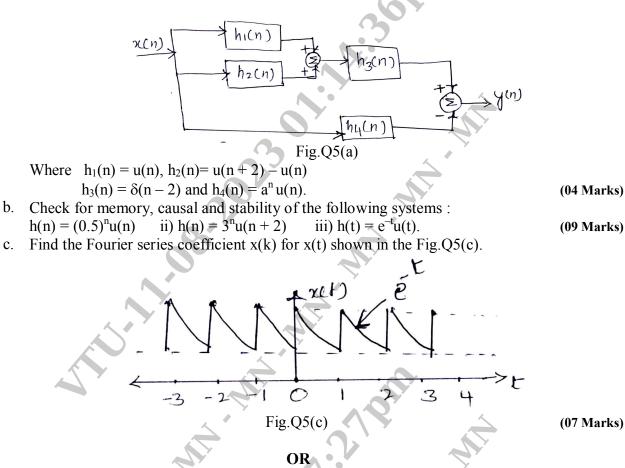


Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8 = 50, will be treated as malpractice. Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.

1 of 3

Module-3

5 a. Find the overall impulse response of the system shown in the Fig.Q5(a).



- 6 a. Find the step response of a system whose impulse response is given by $h(n) = (1/2)^n u(n-3)$. (08 Marks)
 - b. Find the complex Fourier coefficients for x(t) given below : $x(t) = \cos\left(\frac{2\pi t}{3}\right) + 2\cos\left(\frac{5\pi t}{3}\right).$ (06 Marks)
 - c. Find the step response of the system whose impulse response is given by $h(t) = e^{-3t}u(t)$. (06 Marks)

<u>Module-4</u>

7 a. Find the DTFT of a signal $x(n) = a^n u(n)$. Also find the magnitude and phase angle. (08 Marks) b. Find the Fourier transform of a rectangular pulse described below :

$$\mathbf{x}(t) = \begin{bmatrix} \bullet & 1, & |t| < \mathbf{a} \\ \bullet & 0, & |t| > \mathbf{a} \end{bmatrix}$$

Also find magnitude and phase spectrum.

(12 Marks)

OR

- 8 a. Find the Fourier transform of a signal $x(t) = e^{-at}u(t)$. Also calculate its magnitude and phase angle. (06 Marks)
 - b. State and prove the following properties of DTFT
 i) Linearity ii) Time shift iii) Frequency differentiation. (09 Marks)
 - c. Using the properties of Fourier transforms find the Fourier transform of the signal : $x(t) = sin(\pi t) e^{-2t} u(t).$ (05 Marks)

2 of 3

- Find the z transform or a signal $x(n) = 3^n u(n)$. Also plot RoC with poles and zeros. 9 a.
 - Give the significance of the properties of RoC. b.
 - Using the properties of Z transform find the Z transform of the signal $x(n) = n a^{n-1} u(n)$. c.

(06 Marks)

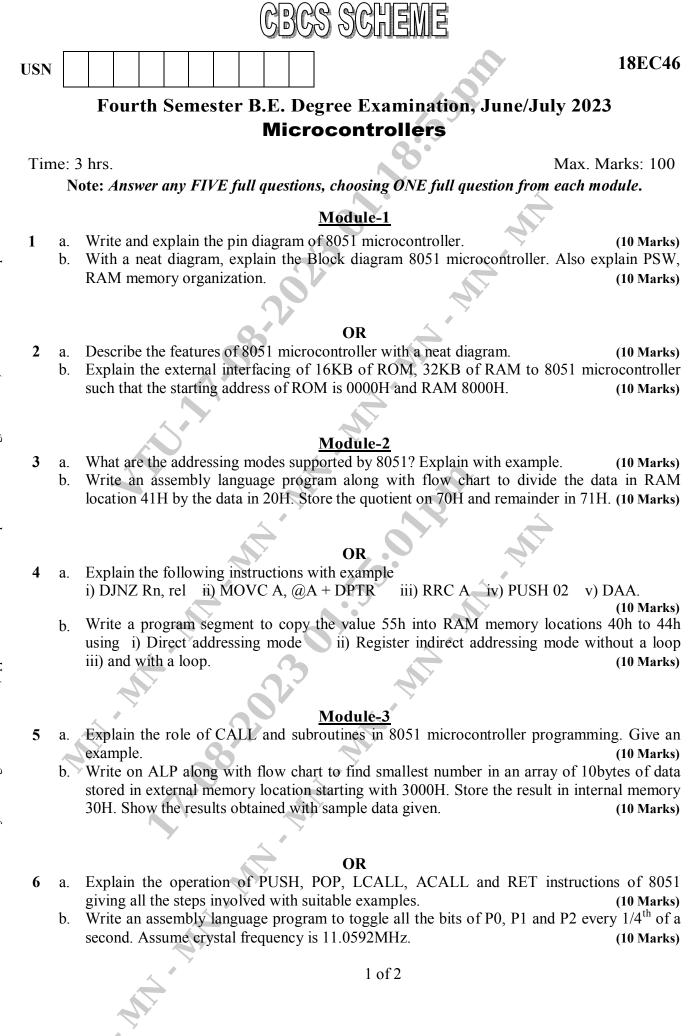
(06 Marks)

(08 Marks)

(06 Marks)

OR •

- State and prove the following properties of Z transform 10 a.
 - Linearity i)
 - Time shift ii)
 - iii) Time reversal.
 - b. Find the inverse Z transform of x(z) using partial fraction expansion approach, $x(z) = \frac{z+1}{3z^2 - 4z + 1}; RoC|z| > 1.$ (06 Marks)
 - Using power series expansion technique find the inverse Z transform of the following x(z): С.
 - i) x(z) =RoC|z| < ii) x(z RoC|z| (08 Marks) 3 of 3



Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice. Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.

(04 Marks)

(06 Marks)

(05 Marks)

Module-4

- 7 a. Explain TMOD register format of 8051.
 - b. Explain MODE-1 programming of timers in 8051.
 - c. Write an ALP to generate square wave of frequency 1KHz on P1.3. Assume crystal frequency, XTAL = 22MHz. User Timer 1 in mode 1. (10 Marks)

OR

- 8 a. Write an 8051 program to transfer "YES" serially at 9600 baud, 8 bit data, 1 stop bit, do this continuously. (05 Marks)
 - b. Explain SCON register with its bit pattern.
 - c. Write the steps required for programming 8051 to transmit and receive the data serially and what is the role of PCON register in serial communication. (10 Marks)

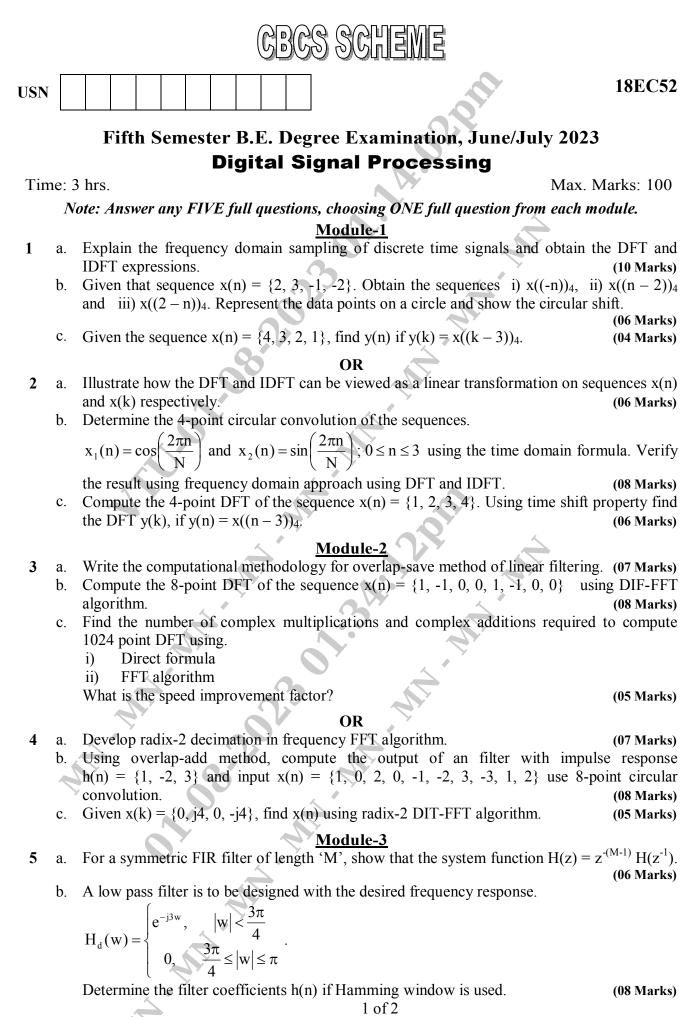
Module-5

- 9 a. Assume that the INTI pin is connected to a switch that is normally high. Whenever it goes low, it should turn on the LED. The LED is connected to P1.3 and is normally off. When it is turned on it should stay on for a fraction of a second. As long as the switch is pressed low, the LED should stay on. Write on ALP for this. (05 Marks)
 - b. Write a program in which the 8051 reads data from P1 and writes it to P2 continuously; while giving a copy of it to the serial comport to be transferred serially. Assume that XTAL = 11.0592MHz. Set the baud rate at 9600. (05 Marks)
 - c. Explain the structure of Interrupt Priority (IP) and Interrupt Enable (IE) SFR. (10 Marks)

OR

- 10 a. Explain DAC interface with diagram and also write a program to generate stair case waveform. (10 Marks)
 - b. Explain stepper motor interface with diagram and also write C program to monitor the status of switch and rotate clockwise if status of switch is zero and anticlockwise if status of switch is one. (10 Marks)

2 of 2



Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8=50, will be treated as malpractice. Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.

c. Realize the FIR filter for the following impulse responses:

i)
$$h(n) = \delta(n) + \frac{1}{4}\delta(n-1) - \frac{1}{8}\delta(n-2) - \frac{1}{8}\delta(n-3) + \frac{1}{4}\delta(n-4) + \delta(n-5).$$

ii)
$$h(n) = \left(\frac{1}{2}\right)^{n} [u(n) - u(n-4)].$$
(06 Marks)
OR

- 6 a. Obtain the magnitude and phase response function of the rectangular window function $w(n) = \begin{cases} 1, & n = 0, 1, & M - 1 \\ 0, & \text{otherwise} \end{cases}$ (06 Marks)
 - b. Obtain the filter coefficients h(n) for a high pass filter with the following desired frequency response,

$$H_{d}(w) = \begin{cases} 0, & |w| < \frac{\pi}{4} \\ e^{-j^{2}w}, & \frac{\pi}{4} \le |w| \le \pi \end{cases}$$
 (08 Marks)

c. Given the FIR filter with the difference equation y(n) = x(n) + 2x(n-1) + 3x(n-2) + 2x(n-3). Obtain the lattice realization. (06 Marks)

Module-4

- 7 a. Obtain the mapping relation between s-plane and z-plane for the bilinear transformation. List the general mapping properties. (08 Marks)
 - b. Given an analog filter with transfer function $H(s) = \frac{5}{s+5}$ convert it into the digital filter transfer function and obtain the difference equation when a sampling period T = 0.05 sec. (06 Marks)
 - c. Realize the following digital filter using direct form-II $H(z) = \frac{0.5z^2 + z + 0.5}{z^2 + 0.5z + 0.4}$. (06 Marks)

OR

- 8 a. List the analog low pass prototype transformations to different filter types and illustrate with the corresponding frequency responses. (08 Marks)
 - b. Design a digital low pass Butterworth filter with the following specifications. 3dB attenuation at the passband frequency 1.5kHz, 10dB stopband attenuation at the frequency 3kHz and sampling frequency of 8000Hz. Draw the direct form-II structure. (12 Marks)

Module-5

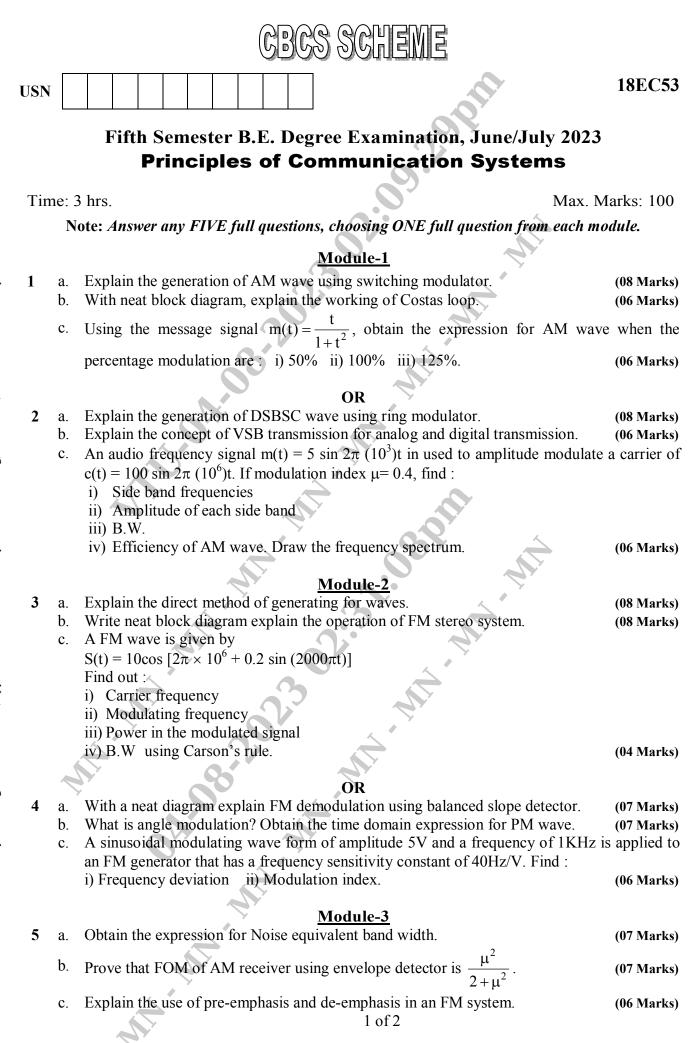
- 9 a. With a neat diagram, explain the Harvard architecture used in DS-processor. Draw the execution cycle. (07 Marks)
 - b. Illustrate the operation of circular buffers for four data samples and show the equivalent FIFO structure. (07 Marks)
 - c. Convert the following decimal numbers to the floating point numbers using 4 bit exponent and 12 bit mantissa. i) 0.64×2^{-2} ii) -0.64×2^{5} . (06 Marks)

OR

- 10 a. With a neat diagram, explain the basic architecture of TMS320C54 \times family DS processor. (12 Marks)
 - b. Perform the following:
 - i) Find the signed Q-15 representation of 0.16.
 - ii) Convert the Q-15 signed numbers to decimal
 - I. 0.100011110110010
 - II. 1.110101110000010

(08 Marks)

* * * * * 2 of 2

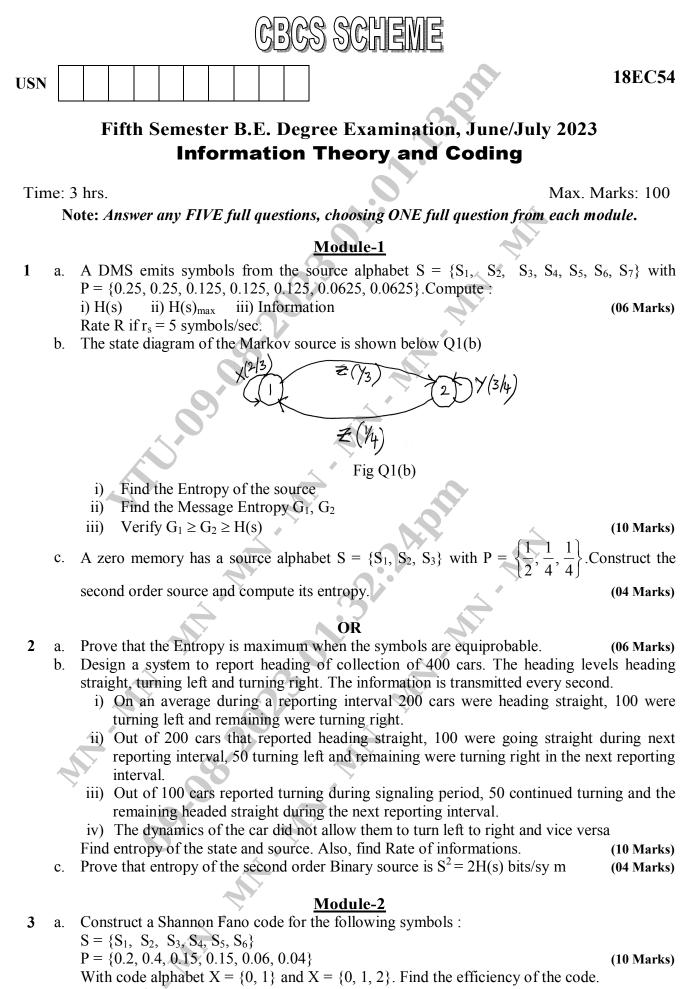


2. Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8=50, will be treated as malpractice. Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.

18EC53

- OR Prove that FOM as a DSBSC receiver in ONE. 6 a. (08 Marks) Define : b. i) Shot Noise ii) Thermal Noise iii) White Noise. (06 Marks) Write neat block diagram explain the FM threshold reduction. C. (06 Marks) Module-4 What are the advantages of digital signal transmission over analog signal transmission? 7 a. (04 Marks) State and prove the sampling theorem for low pass signals. b. (08 Marks) c. A signal $m(t) = 10 \cos(20\pi t) \cos(200\pi t)$ is sampled at the rate of 250 samples/second. i) Sketch the spectrum of sampled signal ii) Specify the cut off frequency for the ideal reconstruction filter so as to recover m(t) from $m_{f}(t)$ iii) Specify the Nyquist rate for the signal m(t). (08 Marks) OR Explain the generation of PAM signals with neat block diagram. 8 a. (08 Marks) b. With neat block diagram, explain the generation of PPM signal. (08 Marks) Write short notes on TDM with neat block diagram. C. (04 Marks) Module-9 Prove that $(SNR)_{0dB} = 1.8 + 6n$ for an uniform quantizer. a. (08 Marks) With neat block diagram, explain the construction and regeneration of PCM signal. b. (08 Marks) Write a short note on VOCODER. c. (04 Marks) OR Explain the construction of Delta modulation signal and explain its disadvantages. 10 a. (08 Marks) Explain how digitization of video and MPEG is achieved with relevant diagram. b. (07 Marks) C.
 - To transmit a bit sequence 10011011. Draw the resulting wave form using :
 i) Unipolar signaling.
 - ii) Polar signaling.
 - iii) Rectangular RZ type.
 - iv) Bipolar RZ.
 - v) Manchester.

(05 Marks)



Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8=50, will be treated as malpractice. Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.

b. A discrete memory less source has an alphabet of six symbols with probability statistics as given below :

Symbols	•••	А	В	С	D	Е	F
Р	•••	0.3	0.25	0.20	0.12	0.08	0.05

i) Construct the Huffman code by moving combined symbols as high as possible. Compute efficiency and variance

ii) Construct the Huffman trainary code by moving symbols combined as high as possible.

OR

4 Test whether the following code is a prefix code : a.

Α	1			
В	0	1		
A B C D	0 0	0	1	
D	0	0	0	1

(04 Marks)

(10 Marks)

Encode the symbols using Shannon encoding algorithm and compute the coding efficiency b. and variance for the following symbol set :

$$X = \{x_1, x_2, x_3, x_4, x_5\}$$

$$\mathbf{P} = \left\{\frac{5}{16}, \frac{1}{4}, \frac{3}{16}, \frac{1}{8}, \frac{1}{8}\right\}$$

(10 Marks)

- A DMS has an alphabet C. $S = \{s_1, s_2, s_3, s_4, s_5, s_6\}$

 - $\mathbf{P} = \left\{\frac{1}{12}, \frac{1}{8}, \frac{1}{12}, \frac{1}{8}, \frac{1}{3}\right\}$

{0, 1, 2}. Compute coding efficiency. Construct Huffman code for the code alphabet X =(06 Marks)

Module-3

Compute Entropy function H(x), H(y) H(xy), H(x/y), H(y/x), Data transmission rate and 5 a. 0.15 0 0 0.15 0 0.2 0.15 0 channel capacity, given $\tau = 0.1 \text{ sec/sym}$ and P(xy) =(07 Marks) 0 0 0.1 0.05 0.1 0.1 0 0

Compute the channel capacity for the channel given below :

$$P(y/x) = \begin{bmatrix} 0.6 & 0.2 & 0.2 \\ 0.2 & 0.6 & 0.2 \\ 0.2 & 0.2 & 0.6 \end{bmatrix}. \text{ Given } r_s = 1000 \text{ sym/sec.}$$
(05 Marks)

Derive an expression for the channel capacity of a Binary Erasure channel. c. (08 Marks)

OR

Prove that Mutual information is always positive. 6 a. (06 Marks) Compute the channel capacity for the channel with $r_s = 1000$ sym/sec and b. 0.6 0.4 P(y/x) =(06 Marks) 0.7 0.3

c. A Binary channel has the following characteristics :

$$P(y/x) = \begin{bmatrix} \frac{2}{3} & \frac{1}{3} \\ \frac{1}{3} & \frac{2}{3} \end{bmatrix} P(x) = \begin{bmatrix} \frac{3}{4} & \frac{1}{4} \end{bmatrix}$$

Compute :

- i) Mutual information
- ii) Channel capacity if $r_s = 100$ sym/sec.

(08 Marks)

Module-4

7 a. For a (6, 3) Linear Block code, the check bits are related to the message bits as per the equations given below :

$$C_4 = d_1 + d_2$$
; $C_5 = d_1 + d_2 + d_3$; $C_6 = d_2 + d_3$

- i) Obtain the Generator Matrix G.
- ii) Find all possible code words.
- iii) Find H and H^{T} .
- iv) Computer syndrome if there is an error in the 3rd bit of a transmitted codeword [110 001] and show how it can be corrected. (10 Marks)
- b. For a (6, 3) cyclic code find the following :
 i) g(x) ii) G in systematic form iii) find all possible code words. (06 Marks)
- c. For a (7, 3) Hamming code with $g(x) = 1 + x + x^2 + x^4$, design a suitable encoder to generate systematic cyclic codes. (04 Marks)

OR

- 8 a. Prove that C. $H^T = 0$ there by show that S = E. H^T
 - b. A (7, 4) cyclic code has the generator polynomial $g(x) = 1 + x + x^4$. Design a syndrome computation circuit and verify the circuit for the message polynomial $d(x) = 1 + x^3$.
 - c. For a (7, 4) Linear Block code the syndrome is given by
 - $S_1 = r_1 + r_2 + r_3 + r_5$

 $S_2 = r_1 + r_2 + r_4 + r_6$

 $S_3 = r_1 + r_3 + r_4 + r_7$

- i) Find G and H matrix
- ii) Draw the Encoder and syndrome computation circuit.

(07 Marks)

(07 Marks)

(10 Marks)

(06 Marks)

Module-5

- 9 a. Consider (3, 1, 2) convolutional encoder with g(1) = (110), g(2) = (101), g(3) = (111)
 - i) Write the Encoder circuit.
 - ii) Write the state transition table.
 - iii) Write the state diagram.
 - iv) Write the code tree.

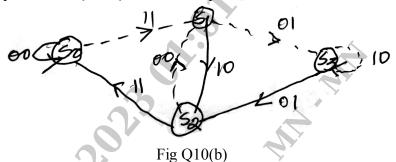
b. For a (2, 1, 3) convolutional encoder with $g^1 = (1101)$, $g^2 = (1011)$

- i) Find the constraint length.
- ii) Find the rate efficiency.
- iii) Find the codeword for the message sequence (11101) using matrix and frequency domain approach. (10 Marks)

(08 Marks)

OR

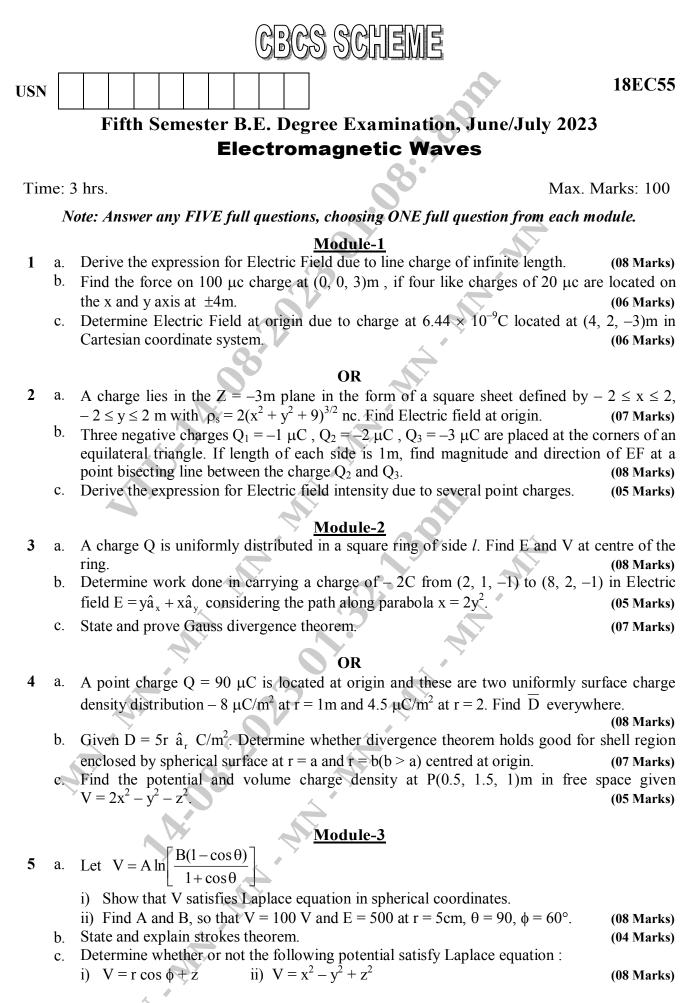
- 10 a. Explain Viterbi Decoding algorithm with an example.
 - b. For the State show below with $S_0 = 00$, $S_1 = 10$, $S_2 = 01$, $S_3 = 11$, draw the trellis diagram. For the input sequence $m = \{1 \ 0 \ 1\}$ trace the output.



(06 Marks)

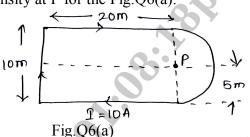
- c. Define the following distance properties of convolution codes
 - i) Minimum free distance
 - ii) Column distance function
 - iii) Minimum distance

(06 Marks)



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6 a. Find the magnetic field intensity at P for the Fig.Q6(a)



(08 Marks)

- There exist a potential of V = -2.5V on the conductor of 0.02m and V = 15V at r = 0.35m. b. (07 Marks) Determine E and D by solving Laplace equation in spherical coordinates.
- If the magnetic field intensity in region H = $(3y 2)\hat{a}_{x} + 2x\hat{a}_{y}$. Find current density. C.

(05 Marks)

(05 Marks)

Module-4

- 7 For region1, $\mu_1 = 4\mu$ H/m and for region2, $\mu_2 = 6\mu$ H/m. The regions are separated by Z = 0 a. plane. The surface current density at the boundary is $K = 100 \hat{a}_x A/m$. Find B_2 if $B_1 = 2\hat{a}_x - 3\hat{a}_y + \hat{a}_z mT$ for Z = 0. (08 Marks)
 - b. A circular conducting loop of radius 40cm lies in xy plane and has a resistance of 20Ω . If magnetic flux density is $B = 0.2 \cos (500t) \hat{a}_x + 0.75 \sin(400t) \hat{a}_y + 1.2 \cos(314t) \hat{a}_z$. Find induced current in Loop. (07 Marks)
 - c. Explain Lorentz force equation

b.

OR

A conductor of length 2.5m in Z = 0 and x = 4m carries a current of 12A in $-\hat{a}_{y}$ direction. 8 a. Calculate uniform flux density in region, if force on the conductor is 12×10^{-2} N in direction

- $\frac{-\hat{a}_x + \hat{a}_z}{\sqrt{2}}$ by (07 Marks) Explain Magnetization and Permeability. (07 Marks)
- Explain force between differential current elements with equation. C. (06 Marks)

Module-5

Given $H = H_m e^{j(wt + \beta z)} \hat{a}$, A/m in free space. Find E. 9 a. (07 Marks) Derive the wave equation for vector E and H field in conducting medium. b. (08 Marks) Prove that $\nabla \times \vec{E}$

(05 Marks)

(07 Marks)

OR

- 10 Discuss the propagation of uniform plane wave in good conductor and explain skin depth. a.
 - (08 Marks) Determine α , β , γ , v, λ , η for damp soil at frequency of 1 MHz given that $\varepsilon_r = 12$, $\mu_r = 1$, b. and $\sigma = 20 \text{m} \text{ v/m}$. (05 Marks)
 - Find the Amplitude of displacement current density in free space within large power C. distribution
 - $H = 10^{6} \cos(377t + 1.256 \times 10^{-6}z)\hat{a},$



18EC56

Fifth Semester B.E. Degree Examination, June/July 2023 Verilog HDL

Time: 3 hrs.

USN

1

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

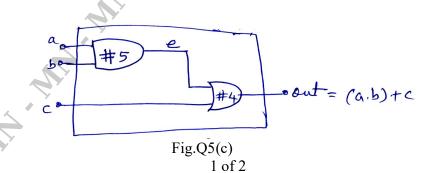
<u>Module-1</u>

1	a.	Explain typical design flow for designing VLSI IC circuits with a neat flow chart.	(10 Marks)
	b.	Explain top-down design methodology and bottom-up design methodology.	(06 Marks)
	c.	Explain trends in HDL's.	(04 Marks)
		OR	
2	a.	Explain design hierarchy by taking 4-bit ripple carry counter.	(08 Marks)
	b.	Define the following terms with examples "	
		i) Module	
		ii) Instances	
		iii) Instance name.	(06 Marks)
	c.	Explain the different levels of abstraction used for programming in verilog.	(06 Marks)
		Module-2	
3	a.	With a neat block diagram, explain the components of verilog module.	(08 Marks)
	b.	Explain \$display, \$monitor, \$finish and \$stop system tasks with examples.	(08 Marks)
	c.	How to write comments in verilog HDL, explain with examples.	(04 Marks)
		OR	
4	a.	Explain the following data types of with an examples :	
		i) Nets	
		ii) Registers	
		iii) Integers	
		iv) Parameters.	(08 Marks)

IV) Parameters.(08 Marks)b. Write verilog description of SR latch. Also write stimulus code.(08 Marks)c. With an example, explain hierarchical names.(04 Marks)

Module-3

- 5 a. What are Rise, Fall and Turn-off delays? How they are specified in verilog. (06 Marks)
 - b. Write a verilog dataflow level of abstraction for 4 to 1 multiplexer using conditional operator. Also write stimulus code. (08 Marks)
 - c. Design a gate level module according to the logic diagram given Fig.Q5(c). Write stimulus code delay.



(06 Marks)

- Develop a gate-level verilog code for 4-bit ripple carry adder from 1-bit full adder. What is 6 a. the output if A = 1010, B = 1100 and $c_{in} = 0$ at t = 0. (10 Marks)
 - b. What would be the output of the following :
 - a = 4'b0111, b = 4'b1001
 - i) &b
 - ii) a<<2
 - iii) $\{a, b\}$
 - iv) $\{2\{b\}\}$
 - a^b v)
 - vi) ab
 - a & b vii)
 - viii) $\sim a$.

c. Declare following variables in Verilog,

- i) A 8-bit vector called a in
- ii) An integer called count.

(08 Marks)

(02 Marks)

(06 Marks)

Module-4

- Discuss sequential and parallel blocks with examples. 7 a. (08 Marks)
 - Write a verilog behavionral description of 8 : 1 multiplexer using case statement. b. (06 Marks)
 - Illustrate the use while loop and repeat loop with examples. c. (06 Marks)

OR

8 Explain blocking and non-blocking assignment statements with relevant examples.(08 Marks) a.

- Write verilog behavioral description of 4-bit binary counter. b. (06 Marks)
- Write the verilog behavioral description of Dflip flap. c.

Module-5

- 9 Define the term logic synthesis. With a neat flow-chart explain computer - Aided logic a. synthesis process. (10 Marks)
 - b. What will the following statement translate to when run on a logic synthesis tool, assign y = (a&b) | (c&b) where y, a, b, c and d are 3 – bit vectors
 - i)

ii) if(s)

out = i1; else out = i0;

(10 Marks)

(10 Marks)

(10 Marks)

OR

10 With neat flow diagram explain synthesis design flow. a.

- b. Write a notes on :
 - i) Assign and deassign
 - ii) Overriding parameters.

USN

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. 2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

3

Sixth Semester B.E. Degree Examination, June/July 2023 **Digital Communication**

CBCS SCHEME

Time: 3 hrs.

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

Determine the Hibert transform of rectangular pulse : 1 a.

> $\frac{1}{2} \le t \le \frac{1}{2}$ rect(t) =0, otherwise

- Express band pass signal S(t) in canonical form. Also derive the schemes for obtaining in b. phase and quadrature components of the band pass signal S(t) and vice-versa. (08 Marks)
- Explain with necessary equations, the time-domain procedure for computational analysis of c. a band pass system driven by a band pass signal. (08 Marks)

OR

Consider a real base band signal $m(t) = 4 \cos(2t) - 6 \sin(3t)$ and a carrier signal 2 a. c(t) = cos(100t). Determine a band pass signal s(t), analytic signal $s_t(t)$ and complex

envelope $\tilde{s}(t)$.

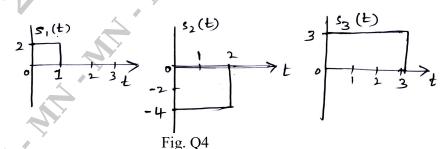
- b. Draw the power spectra of :
 - i) NRZ polar signal
 - ii) Manchester signal.
- Illustrate HDB3, B8ZS and B3ZS signaling schemes and mention its applications. (08 Marks) c.

Module-2

Obtain the maximum likelihood decision rule for the signal detection problem. (10 Marks) a. Derive the expressions for mean and variance of the correlator outputs. Also show that the b. correlator outputs are statistically independent. (10 Marks)

OR

Using the Gram-Schmidt orthogonalization procedure, find a set of orthonormal basis 4 functions to represent the three signals $S_1(t)$, $S_2(t)$ and $S_3(t)$ shown in Fig.Q4(a). Also express each of these signals interms of the set of basis functions.



With a neat diagram, explain the correlation receiver. b.

(10 Marks) (10 Marks)

18EC61

Max. Marks: 100

(08 Marks)

(04 Marks)

(04 Marks)

(04 Marks)

(10 Marks)

Module-3

- With necessary expressions and block diagrams, explain the generation and coherent 5 a. detection of QPSK signals. Also mention the shortcomings of QPSK and solution for the same. (10 Marks)
 - b. Define bandwidth efficiency. Tabulate and comment on the bandwidth efficiency of M-ary (04 Marks) PSK signals for different values of M.
 - c. What is the advantage of M-ary QAM over M-ary PSK system? Obtain the constellation of QAM for M = 4 and draw signal space diagram. (06 Marks)

OR

- Derive an expression for probability of error of BFSK technique. Also draw the black 6 a. diagrams of BFSK transmitter and coherent BFSK receiver. (10 Marks)
 - With a neat block diagram, explain the generation and optimum detection of DPSK signals. b. (10 Marks)

Module-4

- With a neat block diagram, explain the digital PAM transmission through band limited base 7 a. band channels. Also obtain an expression for inter symbol interference. (10 Marks)
 - b. Explain the need for precoder in a duobinary signaling. Consider a binary sequence 111010010001101 is given as an input to the pre coder whose output is used to modulate a duobinary transmitting filter. Obtain the pre coded sequence, transmitted amplitude levels, the received signal levels and the decoded sequence. (08 Marks) (02 Marks)
 - c. State the Nyquist condition for zero ISI.

OR

- What is a zero forcing equalizer? With a neat block diagram, explain the operation of linear 8 a. transversal filter. (08 Marks)
 - Explain the design of band limited signals with controlled ISI. b. (08 Marks)
 - Write a note on eye diagram. c.

Module-5

- With a neat diagram, explain the model of a spread spectrum digital communication system. 9 a. (08 Marks)
 - Explain the generation and demodulation of direct sequence spread spectrum signals with b. necessary equations and block diagram. (08 Marks)
 - c. A direct sequence spread spectrum signal is designed so that the power ratio PR/PN at the intended receiver is 10^{-2} . If the desired $E_b/N_0 = 10$ for acceptable performance, determine the maximum value of the processing gain. (04 Marks)

OR

- With a neat bock diagram, explain the frequency hopped spread spectrum. 10 a. (06 Marks)
 - With a neat diagram, explain the IS 95 reverse link. b.
 - Write a note on law detectability signal transmission as an application of DSSS. c. (04 Marks)

Sixth Semester B.E. Degree Examination, June/July 2023 **Embedded Systems**

Time: 3 hrs.

USN

1

2

3

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- List the different registers of ARM CORTEX-M3 and mention their use. Explain the use of a. link register with an illustration. (08 Marks)
 - b. Explain Program Status Register (PSR) configuration. Illustrate how to access different subdivisions of PSR. (06 Marks)
 - Explain exceptions and interrupts of ARM CORTEX-M3. c.

OR

- Explain the operation modes of CORTEX-M3 with a block diagram. (08 Marks) a.
 - Explain CORTEX-M3 stack implementation for push and pop operations. (06 Marks) b.
 - Explain reset sequence of CORTEX-M3 why LSB of reset vector address is set to 1. c.

(06 Marks)

(06 Marks)

Module-2

- Explain following instruction of ARM CORTEX-M3 with suitable illustration: a. (i) BIC (ii) SBFX (iii) REVSH (iv) LDRH (08 Marks)
 - Write an assembly language program to find sum of all even numbers in a given array of 10 b. numbers. (06 Marks)
 - Explain conditional execution using IT instructions with an example. (06 Marks) c.

OR

- Explain all shift and rotate instructions of CORTEX-M3 with illustration. How rotate left 4 a. operation can be implemented? (10 Marks)
 - b. Write an assembly language program to determine the parity of a 32 bit number. If even parity store 00h in a memory location otherwise store FFh in the location. (06 Marks)
 - Assume R0 = 0X12345678, R1 =0XFEDCBA12. Write the result after executing following instructions:
 - R0, #8, #16 (i) BFC.W
 - UBFX.W R0, R1, #4, #8 (ii)
 - BFI.W R1, R0, #8, #16 (iii)
 - (iv) REVSH R1, R0

Module-3

- Explain Big Endian and little Endian operation and give examples. 5 (06 Marks) a. With a diagram, explain SRAM cell implementation and its working. Give comparison b. between SRAM and DRAM cells. (08 Marks)
 - Explain the sequence of operation for communicating with an I2C slave device. (06 Marks) c.

OR

(04 Marks)

18EC62

Max. Marks: 100



18EC62

(06 Marks)

- 6 Give comparison between RISC and CISC. a.
 - With a circuit diagram, explain how input and output circuits of a processor can be isolated. b. (06 Marks)
 - Explain SPI Bus interfacing and sequence of operation for communicating with a SPI c. device. (08 Marks)

Module-4

Explain characteristics of an embedded system with examples for each. 7 (06 Marks) a. Explain state machine model (FSM) by considering automatic seat belt warning system. b.

(08 Marks)

Discuss advantages and drawbacks of super loop based firmware design approach. (06 Marks) c.

OR

- Explain any six nonoperational quality attributes. Explain product life cycle curve. (10 Marks) 8 a.
 - b. Design an automatic tea/coffee vending machine based on FSM model for the following requirement: The tea/coffee vending is initiated by user inserting a 5 rupees coin. After inserting coin, the

user can either select 'Coffee' or 'Tea' or press 'Cancel' the order and take back the coin.

(06 Marks)

(04 Marks)

Explain the assembly language to machine language conversion process with block diagram. (04 Marks)

Module-5

- Explain monolithic and micro kernels with suitable example for each. (06 Marks) a. (08 Marks)
 - Explain task, process and threads. b.

9

Three processes with process IDs P1, P2, P3 with estimated completion time 10, 5, 7 ms c. respectively enter the ready queue together in order P1, P2, P3. Calculate waiting time and turn around time for each process and average waiting time and TAT. (Assume there is no I/O waiting for the processes) (06 Marks)

OR

- Explain different conditions that favour deadlock. Explain techniques to detect and prevent 10 a. deadlock. (08 Marks)
 - With a block diagram, explain the concept of counting semaphore. Give real world example. b. (08 Marks)
 - Explain the advantages of simulation based debugging. c.

18EC63

(06 Marks)

(05 Marks)

Sixth Semester B.E. Degree Examination, June/July 2023 Microwave and Antenna

CBCS SCHEME

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

<u>Module-1</u>

- 1 a. List the limitations of conventional microwave tubes? Discuss how these limitations can be reduced? (06 Marks)
 - b. A transmission line has following parameters :
 - $R = 2\Omega/m$, G = 0.5mho/m, f = 1 GHz, L = 8nH/m, c = 0.23pF. Calculate :
 - i) The characteristic impedance
 - ii) The propagation constant.
 - c. Explain Suflex Klystron oscillator with neat block schematic and mode curves. (08 Marks)

OR

- a. Derive the equation of transmission line and discuss its possible solution. (10 Marks)
 - b. List the characteristics of smith chart.
 - c. A certain transmission line has a characteristics impedance of 75 + j0.01ohms and is terminated in a load impedance of 70 + j50ohms. Compute the reflection coefficient, transmission coefficient and standing wave ratio.

Module-2

- 3 a. Derive the S-matrix representation for multiport network and using this derive the S-matrix solution for E-plane T Junction. (10 Marks)
 - b. Explain different types of attenuators, with its neat schematic diagram. (10 Marks)

OR

- 4 a. List the characteristics of magic T when all the ports are terminated with matched load. Also derive the S – matrix relation along with its schematic. (10 Marks)
 - b. In a H plane T Junction, compute power delivered to the loads of 40ohms and 60ohms connected to arms 1 and 2 when a 10MW power is delivered to the matched port 3. Choose characteristic impedance $Z_0 = 50\Omega$. (06 Marks)
 - c. Example briefly phase shifter.

Module-3

- a. A certain micro strip line has the following parameters : $\varepsilon_r = 5.23$, h = 7 mils, t = 2.8 mils and w = 10mils. Calculate the characteristic impedance of the line. (04 Marks)
- b. Define the following terms related to antenna with relevant equation :
 - i) Directivity
 - ii) Field pattern
 - iii) Beam efficiency.
- c. Determine the directivity of the system if radiation intensity is given by $U = U_m \sin \theta \sin^2 \phi$. When $0 \le \phi < \pi$ and $0 \le \phi < \pi$, using :
 - i) Exact method and
 - ii) Approximate method.

(10 Marks)

(06 Marks)

(04 Marks)

2

5

(10 Marks)

(10 Marks)

- 6 a. A lossless parallel strip line has a conducting strip width W. The substrate dielectric separating the two conducting strip has a relative dielectric constant ε_{rd} of 6 and a thickness d of 4mm calculate :
 - i) the squired width w of the conducting strip in order to have a characteristic impedance of 50Ω .
 - ii) Strip line capacitance
 - iii) The strip line inductance

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- iv) Phase velocity of the have in parallel strip line.
- b. Explain radio communication link and derive its relation interms of received and transmitted power. (06 Marks)
- c. Compute the power received by the receiver antenna kept at a distance of 100km by transmitter radiating at 3MHz. Assume $G_T = 40$ and $G_R = 15$ and $P_T = 1000$ KW. (04 Marks)

Module-4

- 7 a. Obtain the field pattern for two point source situated symmetrically with respect to the origin. Two sources are fed with equal amplitude and equal phase signals. Assume distance between two sources = $\lambda/2$. (10 Marks)
 - b. Derive the expression for radiation resistance of short dipole with uniform current. (10 Marks)

OR

- 8 a. Linear antenna consists of 04 isotropic sources. The distance between element is $\lambda/2$. The power is applied with equal amplitude and in phase. Also compute HPBW and FNBW.
 - b. Starting from electric and magnetic potential obtain the far field components for a short dipole. (10 Marks)

Module-5

9 a. Derive the radiation resistance of circular loop of any radius 'a'. (10 Marks)
b. Find the length L, H – plane aperture and flare angle θ_E and θ_H of pyramidal horn for which E – plane aperture is 10λ. Horn is fed by a rectangular wave guide with TE₁₀ Mode. Assume δ = 0.2λ in E – plane and 0.375λ in H – plane. Also find E – plane, H – plane beam width and directivity. (10 Marks)

OR

10 a. Briefly explain helical antenna with its helical geometry.(06 Marks)b. Explain different types of horn antenna with schematic diagram.(08 Marks)c. Explain the construction details of Yogi-uda array.(06 Marks)



Sixth Semester B.E. Degree Examination, June/July 2023 **Digital System Design Using Verilog**

Time: 3 hrs.

1

Max. Marks: 100

(05 Marks)

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- What are the effects of capacitive loading and propagation delay on signal transitions a. between logic level? (10 Marks)
 - Develop a verilog model for a 7-segment decoder that includes an additional input, b. "BLANK" that overrides the BCD input and causes all segments not to lit. (10 Marks)

OR

Discuss about fixed point numbers and fixed-point representation in verilog. 2 a. (10 Marks) Explain the synchronous timing methodologies. b. (10 Marks)

Module-2

- Design a $16K \times 48$ -bit memory using $16K \times 16$ -bit memory component. 3 a. (08 Marks)
 - Explain flow through and pipelined SSRAM with the help of timing diagram. b. (12 Marks)

OR

- Develop a verilog model of a dual-port $4K \times 16$ bit flow through SSRAM. One port allows 4 a. data to be written and read. While the other port allows data to be read. (10 Marks)
 - b. Determine whether there is an error in the ECC word "000111000100", and if so, correct it. (05 Marks)
 - Discuss about multiport memories.

Module-3

Explain the internal organization of a CPLD, with neat diagram. 5 a. (10 Marks) Explain different types of packaging and circuit boards. b. (10 Marks)

OR^A

- a. Define signal integrity. Discuss ground bounce issue in signal integrity and technique used 6 to reduce ground bounce effect. (10 Marks) (10 Marks)
 - b. Discuss the internal architecture of FPGA.

Module-4

With a neat figure, explain flash ADC and SAR ADC. 7 a. (10 Marks) Discuss about multiplexed buses, with neat figure. b. (10 Marks) OR Explain the following serial interface standards. 8 a. i) RS – 232 ii) I^2C . (10 Marks) Explain the following I/O synchronization techniques: b. i) Polling ii) Interrupts. (10 Marks) 1 of 2

c.

(10 Marks)

(10 Marks)

<u>Module-5</u>

- a. Explain the design flow of hardware/software codesign.
 - b. Explain floor plan, placement and routing of ASIC physical design.

OR

- 10 a. Explain the concepts of scan design and boundary scan.
 - b. Explain Built-In Self Test (BIST) techniques.

9

(10 Marks)

(10 Marks)

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18EC72

Seventh Semester B.E. Degree Examination, June/July 2023 VLSI Design

CBCS SCHEME

Time: 3 hrs.

USN

1

2

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- Implement a 4 : 1 multiplexer using : a.
 - i) Transmission gate
 - ii) Tristate inverters

- (08 Marks)
- b. Realize CMOS compound gate for the function : $Y = \overline{D + A(B + C)}$. (04 Marks)
- With necessary circuit diagram and timing diagram explain the operation of positive edge c. triggered D flip-flop. (08 Marks)

OR

- Draw the circuit diagram of a CMOS inverter and its DC transfer characteristics. Explain a. various region of operation and indicate the voltage levels. Derive the equation for switching threshold. (10 Marks)
 - b. Derive the equation for drain current of a MOSFET in non-saturated and saturated region of operation. (06 Marks)
 - c. Explain the following non-ideal effects of a MOSFET -channel length modulation mobility degradation. (04 Marks)

Module-2

With necessary diagrams explain CMOS n-well fabrication process. 3 (12 Marks) a. Draw the layout of Y = ABC + D and estimate the area. (08 Marks) b.

OR

- With necessary diagrams explain lambda based design rules for wires, contact cuts and 4 a. transistors. (08 Marks)
 - b. Explain MOSFET capacitances in three different regions of operation with necessary diagrams and equations. (06 Marks)
 - c. What is Scaling? Compute drain current, power, current density, power density, Cox for constant field scaling. (06 Marks)

Module-3

- Explain the RC delay model to compute the delay of the logic circuit. Also calculate the 5 a. delay of unit size inverter driving another unit size inverter. (08 Marks)
 - b. With necessary circuit example explain :
 - i) Pseudo nMOS
 - ii) Ganged CMOS.
 - Explain the following CMOS optimization techniques with necessary examples : c. i) Input ordering
 - ii) Asymmetric gates.

(06 Marks)

(06 Marks)

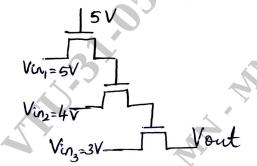
- Analyze the three input NAND gate using Elmore's delay and compute the falling and rising 6 a. propagation delays if the output is loaded with 'h' identical gates. (08 Marks)
 - b. Compute and compare the logical effort and parasitic delay of the following gates with the help of schematic diagram : i) 2 input NOR gate
 - ii) Input NAND gate.

(06 Marks)

Explain Cascade voltage switch logic (CVSL) implement two input OR/NOR gate using c. CVSL. (06 Marks)

Module-4

7 Compute the output voltage Nout in the following pass transistor circuits. Assume a. $V_{tn} = 0.7 V.$



(08 Marks)

Vout

Fig.Q7(a) b. With necessary diagrams and equations explain charge storage and charge leakage in dynamic logic. (06 Marks)

21

c. With necessary circuit diagrams explain resettable latches with i) synchronous reset ii) asynchronous reset. (06 Marks)

OR

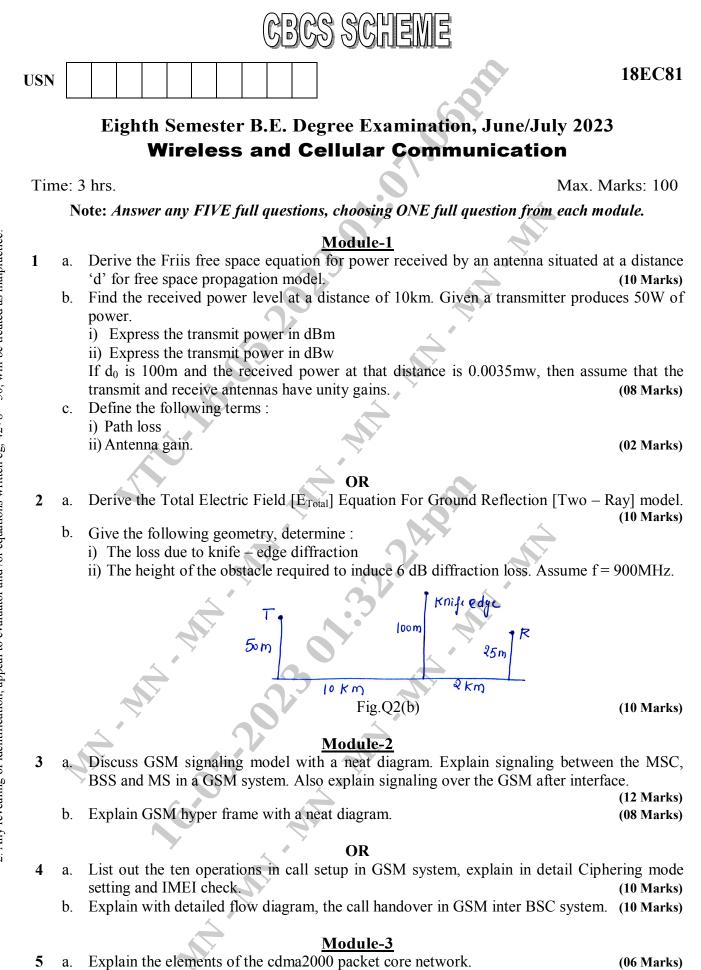
- Explain dynamic logic with an example. Also explain the advantage and limitations of 8 a. dynamic logic. (08 Marks)
 - b. With necessary circuit diagram explain 3 bit dynamic shift register with enhancement load (radio less). (08 Marks)
 - Explain dynamic synchronous CMOS transmission gate logic with necessary diagrams. c. (04 Marks)

Module-5

- With necessary circuit diagram explain the operation of four transistor DRAM cell. 9 a.
 - (06 Marks) Explain the terms : i) controllability ii) obsevability iii) repeatability iv) survivability. b.
 - (08 Marks) Explain full CMOS SRAM cell with necessary circuit topology. c. (06 Marks)

OR

Explain CMOS bridging fault with necessary example. 10 (06 Marks) a. What is a fault model? Explain stuck at fault model with examples. b. (08 Marks) Draw the circuit of 3 bit BILBO register and explain. c. (06 Marks)



Explain various types of CDMA handoff. c.

1 of 2

(08 Marks)

(06 Marks)

2. Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8=50, will be treated as malpractice. Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.

- Explain CDMA access channel probing.

- Explain the major components of a cdma2000 wireless system with details of network 6 a. nodes. (08 Marks)
 - Explain the generation of the CDMA paging channel signal with a relevant diagram. b. (06 Marks)
 - Explain generation of the CDMA reverse traffic channel with a relevant diagram. (06 Marks) C.

Module-4

- Highlight the advantages and disadvantages of OFDM? a. (06 Marks)
 - Explain IP based flat network architecture used in 3GPP evolution. b. (06 Marks)
 - Explain how the data blocks preparation using cyclic prefix are represented in OFDM. C.

(08 Marks)

OR

- 8 What are the multi antenna techniques incorporated to combat multipath fading. a. (06 Marks) (07 Marks)
 - Explain the concept of OFDM with relevant block diagram. b.
 - Describe the feature of SC FDE system. Also compare its performance with OFDM. c.

(07 Marks)

(04 Marks)

Module-5

- Explain with relevant diagram OFDM uplink transmitter/downlink receiver for K users. 9 a. (08 Marks)
 - Compare different OFDMA Rate Adaptive Resource Allocation scheme. Explain the b. maximum sum rate algorithm. (08 Marks)
 - Explain in brief the design principles of LTE. c.

7

OR

- Explain with relevant diagram SC FDMA uplink receiver. Highlight the advantages and 10 a. disadvantages associated with the SC-FDMA. (10 Marks)
 - Explain the proportional rate constraint algorithm and proportional fairness scheduling. b. (10 Marks)

 b. The sole aim of the attacker is to maximize financial gain by attacking computer sy, Identify the attack and further elaborate the different varieties of same. (10 More that the attack and further elaborate the different varieties of same. (10 More that the attack and further elaborate the different varieties of same. (10 More that the attack attack? Explain in detail how active attacks are classified. (10 More that the with real time examples, discuss phishing and pharming. (10 More that the attack attack? Explain in detail how active attacks are classified. (10 More that the with real time examples, discuss phishing and pharming. (10 More that the with real time examples, discuss phishing and pharming. (10 More that the with diagram the step by step operation of SSL record protocol. Explain cae briefly. (10 More that the diagram, explain Secure Shell (SSH) protocol stack. (10 More that and explain IP sec documents. (10 More that and the sec of padding and Anti-Replay service. (10 More that and explain IP sec documents are the working of basic combinations of security associations. (10 More that and attack are the working of basic combinations of security associations. (10 More that an eat diagram, illustrate the profiles of intruder and authorized users. Also dot that an eat diagram illustrate the profiles of intruder and authorized users. Also dot t	USN			18EC82
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Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. 2. Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8 = 50, will be treated as malpractice.

(10 Marks)

OR

- 8 a. Describe the overall taxonomy of software threats (Terminology of Malicious program).
 - b. Explain the anti-virus approaches and also in detail discuss the generations of antivirus software. (10 Marks)

Module-5

- 9 a. Explain the four general techniques that the fire wall use to control access.
 b. Discuss the capabilities which one within the scope of a firewall.
 (05 Marks)
 (05 Marks)
 - c. With a neat diagram, describe the working of packet filtering fire wall.

OR

10a.Discuss the characteristics of Bastion Host.(10 Marks)b.Explain Host based and personal firewalls.(06 Marks)c.Explain the different purposes for which internal fire wall can be used.(04 Marks)

		CBCS SCHEME	
USN			21EC32
		Third Semester B.E. Degree Examination, June/July 2023	5
		Digital System Design Using Verilog	
Tin	ne: í	3 hrs.	farks: 100
	Ν	ote: Answer any FIVE full questions, choosing ONE full question from each mo	odule.
1	a.	Define combinational logic circuit and place the following equation into canonical form,	the proper
		(i) $P = f(a, b, c) = ab + ac + bc$. (ii) $Q = f(a, b, c) = (a + \overline{b})(\overline{b} + c)$	
	h	(iii) $Z = f(a, b, c, d) = (a + \overline{b})(a + \overline{b} + d)$	(10 Marks)
	b.	Find all the prime implicants of the function using Quine-McClusky method. $Z = f(a, b, c, d) = \sum m(7, 9, 12, 13, 14, 15) + d(4, 11)$	(10 Marks)
		OR	
2	a.	Simplify the following expression using K-map. Implement the simplified expression $\sum_{i=1}^{n} (a_i + a_i) = \sum_{i=1}^{n}	
	b.	basic gates only $F = f(a, b, c, d) = \sum m(0, 1, 2, 5, 6, 7, 8, 9, 10, 13, 14, 15)$. Design a logic circuit that has 4 inputs, the output will be high when the maj	(10 Marks
	0.	inputs are high. Use K-map to simplify.	(10 Marks
3	a.	<u>Module-2</u> Implement the following Boolean function using 8 : 1 multiplexer and 4 : 1 multi	plexer.
-		$M = f(a, b, c, d) = \sum m(0, 1, 2, 4, 6, 9, 12, 14)$	(10 Marks
	b.	Explain 4-bit carry look ahead adder with neat diagram and relevant expressions.	(10 Marks
		OR	
4	a. b.	Implement full adder and full subtractor using 74138 decoder. Design 2-bit magnitude comparator.	(10 Marks (10 Marks
		Module-3	
5	a. h	Explain Master Slave JK flip flop with the help of circuit diagram and waveform	
	U.	Design a mod-6 synchronous counter using JK flip flop.	(10 Marks
6	a.	OR Find characteristic equations for SR, T, D and JK flip flop with the help of functi	on table
Ū	b.	Explain four bit binary ripple counter with logic and timing diagram.	(10 Marks) (10 Marks)
	0.		
7	a.	List all the data types available in verilog HDL and explain any three data	types with
	h	examples.	(10 Marks
	b.	Explain various descriptive styles available for hardware modeling using verilog an example.	(10 Marks
		1 of 2	

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. 2 Anv revealing of identification anneal to evaluator and /or equations written eg. 42+8 = 50. will be treated as malbractice.

OR

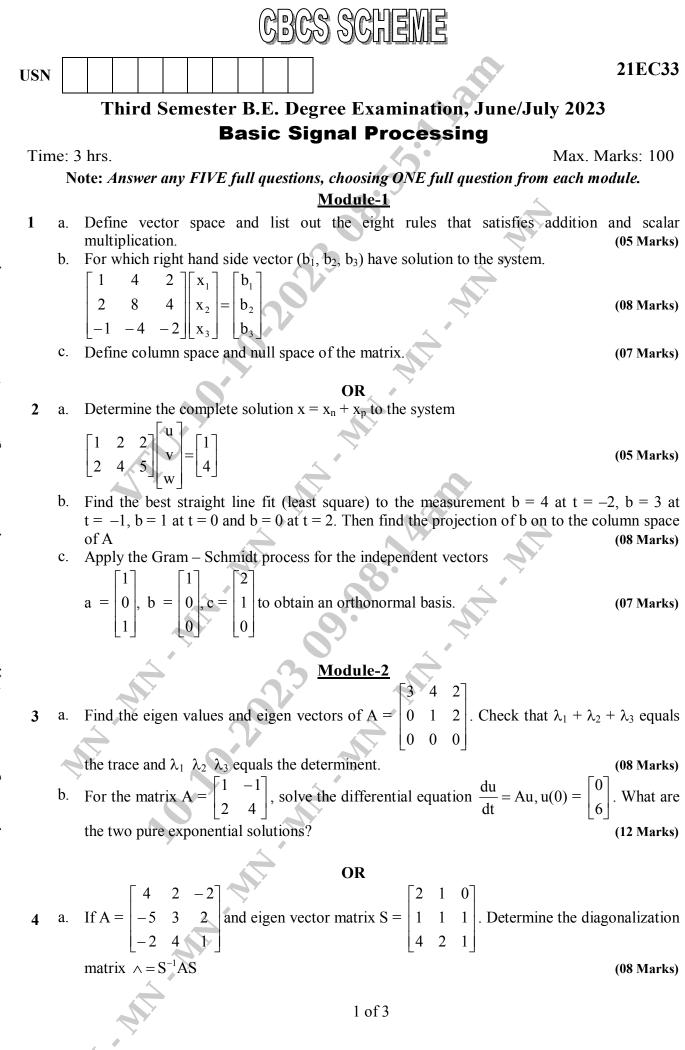
8 a. Explain the different types of logical operators with an example program.
b. Write a full subtractor verilog program using dataflow type of description.
(10 Marks)
(10 Marks)

Module-5

- 9 a. With a neat block diagram, explain the components of a verilog module by highlighting mandatory blocks. (10 Marks)
 - b. Write a verilog behavioural code for 4 to 1 multiplexer using case statement. (10 Marks)

OR

10a. Write a verilog structural code for four bit ripple carry adder.(10 Marks)b. Explain the highlights of structural description with an example.(10 Marks)



	b.	For the matrix $A = \begin{bmatrix} 1 & 2 \\ 3 & 6 \end{bmatrix}$, find the eigen values, eigen vector v_1 , v_2 and $A^T A$. Then find
		u ₁ , u ₂ and recover A using Singular Value Decomposition (SVD).	(12 Marks)
		Module-3	
5	a.	Define signals and systems.	(04 Marks)
C	b.	x(n) = [2, 2, 2, 2, -2, -2, -2, -2]. Sketch i) $x(n-3)$ ii) $x(2n+3)$.	(06 Marks)
		Determine whether the system $y(n) = nx(n)$ is	· · · · ·
	c.	i) Stable	
		ii) Memory	
		iii)Causal	
		iv) Time invariant	
		v) Linear	(10 Marks)
		OR	
6	a.	Sketch the signal $x(n) = u(n + 10) - 2u(n) + u(n - 6)$	
		y(n) = 2n[u(n) - u(n) - 6)]	(10 Marks)
	b.	Sketch the following signals	
		i) $x(2n)$ ii) $x(3n-1)$	
		iii) $x(n) u(1-n)$ if $x(n) = [3, 2, 1, 0, 1, 2, 3]$	(10 Marks)
			· · · · ·
		<u>Module-4</u>	
7	a.	Derive an expression for convolution sum for Linear Time Invariant (LTI) system	
	b.	Compute $y(n) = u(n) * u(n)$ using graphical method.	(08 Marks)
	c.	Compute $y(n) = x(n) * h(n)$, where $x(n) = u(n)$ and $h(n) = \left(\frac{3}{4}\right)^n u(n)$ using graphic	al method.
			(08 Marks)
•		OR OR	
8	a. b.	Show that convolution posses the associative and distributive property. For the impulse response $h(n) = 2u(n) - 2u(n - 5)$. Determine whether t	(08 Marks)
	υ.	i) Memoryless	the system
		ii) Stable	
		iii) Causal	(06 Marks)
	c.	What is step response? Evaluate the step response of the LTI system who	se impulse
		response in $h(n) = \left(\frac{1}{2}\right)^n u(n)$.	(06 Marks)
		Madula 5	

- a. Find the z-transform and mention ROC of the following signals 9

 - Find the 2-transform and men i) x(n) = [1, 2, 3, 4, 0, 7]ii) x(n) = [1, 2, 3, 4, 0, 7]iii) x(n) = [1, 2, 3, 4, 0, 7]

2 of 3

(03 Marks)

- b. Find the z-transform of the signal $x(n) = a^n u (-n-1)$ with ROC diagram. (05 Marks)
- c. Using the properties of the z-transform, find the z-transform of the following signals i) $x(n) = a^n \cos \Omega_0 n u(n)$

ii)
$$x(n) = u(n-2)^* \left(\frac{2}{3}\right)^n u(n)$$
 (12 Marks)

OR

10 a. Using partial fraction expansion method find the inverse z-transform of

$$x(z) = \frac{1 - z^{-1} + z^{-2}}{\left(1 - \frac{1}{2}z^{-1}\right)(1 - 2z^{-1})(1 - z^{-1})} \text{ for}$$

i) ROC 1 < |z| < 2
ii) ROC $\frac{1}{2}$ < |z| < 2
iii) ROC |z| < $\frac{1}{2}$

(08 Marks)

b. A causal system has an input $x(n) = \delta(n) + \frac{1}{4}\delta(n-1) + \frac{1}{\delta}\delta(n-2)$ and output

$$y(n) = \delta(n) - \frac{3}{4}\delta(n-1)$$
. Find the transfer function of the system. (04 Marks)

c. The LTI system is $H(z) = \frac{3-4z^{-1}}{1-3.5z^{-1}+1.5z^{-2}}$. Specify ROC of H(z) and determine h(n) for

the following conditions

- i) The system is stable
- ii) The system is causal
- iii) The system is anticausal

(08 Marks)



Third Semester B.E. Degree Examination, June/July 2023 Analog Electronic Circuits

Time: 3 hrs.

1

2

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- a. Explain the classical biasing for BJTs using a single power supply with circuit and relevant equations. How is bias current stabilized? (08 Marks)
 - b. Design collector-to-base feedback resistor circuit to obtain a dc emitter current of 1mA and to ensure $V_{CE} = 2.3V$. Let $V_{CC} = 10V$ and $\beta = 100$. (04 Marks)
- c. Considering the conceptual circuit of common emitter amplifier, derive the expression for small-signal input resistance between base and emitter resistance. Mention the relation between r_{π} and r_{e} . (08 Marks)

OR

- a. Why biasing by fixing V_{GS} is not a good approach? Explain biasing by fixing V_G and connecting a resistance in the source. (10 Marks)
 - b. Design Drain-to-Gate feedback resistor biasing circuit to operate at a dc drain current of 0.5mA. Assume $V_{DD} = 5V$, $K'_n W/L = 1mA/V^2$, $V_t = 1V$ and $\lambda = 0$. Use standard value for R_D and give actual values obtained for I_D and V_D . (06 Marks)
 - c. A BJT having $\beta = 100$ is biased at a dc collector current of 1mA. Find the value of g_m , r_e and r_{π} . Assume $V_T = 25 \text{mV}$. (04 Marks)

Module-2

- 3 a. Obtain the expression for characteristic parameters of the CS amplifier with circuit diagram and its equivalent circuit. (08 Marks)
 - b. A CS amplifier utilizes a MOSFET biased at $I_D = 0.25$ mA with $V_{OV} = 0.25$ V and $R_D = 20$ K Ω . The device has $V_A = 50$ V. The amplifier is fed with a source having $R_{sig} = 100$ K Ω and a 20-K Ω load is connected to the output. Find R_{in} , A_{vo} , R_o , A_v and G_v . (05 Marks)
 - c. Explain the internal capacitances of a MOSFET and hence draw the high frequency small signal model of MOSFET. (07 Marks)

OR

- 4 a. Find the mid band gain A_M and the upper 3-dB frequency f_H of a CS amplifier fed with a signal source having an internal resistance $R_{sig} = 100K\Omega$. The amplifier has $R_G = 4.7M\Omega$, $R_D = R_L = 15K\Omega$, $g_m = 1mA/V$, $r_0 = 150K\Omega$, $C_{gs} = 1pF$ and $C_{gd} = 0.4pF$. (06 Marks)
 - b. Explain the working of FET based RC phase shift oscillator with circuit diagram. In an RC phase shift oscillator, $R = 200K\Omega$ and C = 200pF. Find the frequency of the BJT-based oscillator. (08 Marks)
 - c. Explain the working of clapp oscillator with a circuit diagram. (06 Marks)

1 of 2

Module-3

- Explain general feedback structure of the feedback amplifier with a signal flow diagram and 5 a. mathematical expressions. (08 Marks)
 - Explain noise reduction with the application of negative feedback in amplifiers. (08 Marks) b.
 - A class B push-pull amplifier is supplied with $V_{CC} = 50V$. The signal brings the collector C. voltage down to $V_{min} = 5V$. The total dissipation from both transistors is 40W. Find the total power and conversion efficiency. (04 Marks)

OR

- Explain transconductance amplifier with a neat block diagram. 6 (06 Marks) a. Explain class-B transformer-coupled amplifier. Prove that the maximum conversion b. efficiency of a class B transformer coupled amplifier is 78.5%. (08 Marks) (06 Marks)
 - Explain class C output stage with a neat diagram. c.

9

Module-4

- Explain inverting amplifier with external offset null circuit and relevant expressions for 7 a. output voltage and closed loop gain. (07 Marks)
 - Explain successive-approximation type A/D converter with a neat diagram. b. (07 Marks)
 - Explain positive small-signal half-wave rectifier circuit with waveforms. (06 Marks) c.

OR

- Explain the working of a second order high pass Butterworth filter with a neat circuit 8 a. diagram and frequency response. Write the relevant design equations. (08 Marks)
 - Design second order low-pass filter at a high cutoff frequency of 1kHz. Choose capacitance b. value 0.0047µF. (05 Marks)
 - Explain the operation of 555 timer as astable multivibrator with relevant expressions. C.

(07 Marks)

Module

- Explain the classification of power electronic convertors. a. (06 Marks) With the help of elementary circuit and static V-I characteristics, explain the three regions of b operation of the SCR. (08 Marks)
- Explain class-A commutation with necessary circuit diagram and waveforms. c. (06 Marks)

OR

- Write a note on basic requirements for the successful firing of a thyristor. 10 a. (04 Marks) b. Explain RC firing circuit with necessary circuit diagram and waveform. Write the relevant design equations. (08 Marks)
 - c. Explain UJT relaxation oscillator with a neat circuit diagram. Derive the expression for frequency of oscillation. (08 Marks)

2 of 2

21EC42

Fourth Semester B.E. Degree Examination, June/July 2023 Digital Signal Processing

GB(GS) S)GHEME

Time: 3 hrs.

1

2

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

<u>Module-1</u>

- a. Define. DFT and IDFT and solve for the 4-point DFT of the sequence x(n) = [0, 1, 2, 3] and also write program to find N-point DFT. (10 Marks)
 - b. Explain the process of frequency domain sampling and reconstruction of discrete time signal. (10 Marks)

OR ____

- a. Summarize multiplication of two DFT properties and also write a program to verify Pasval's theorem. (08 Marks)
 - b. Make use of DFT and IDFT to compute circular convolution of the sequence. x(n) = [2, 3, 1, 1] and h(n) = [1, 3, 5, 3]. (08 Marks)
 - c. The five samples of 8-point DFT X(K) are given X(0) = 0.5, X(1) = -j2, X(4) = X(6) = 0. X(5) = +j2. Make use property to find remaining Samples and also find x(0). (04 Marks)

Module-2

- **3** a. Explain the computational arrangement of 8-point DFT using Radix 2 DIT-FFT algorithm.
 - b. Examine the o/p y(n) = x(n) * h(n) if x(n) = [1, 0] and h(n) = [1, 3, 1] using Radix 2 DIT - FFT algorithm. (12 Marks) (08 Marks)

OR

- 4 a. Examine the output of y(n) of a filter where impulse response h(n) = [3, 2, 1] input sequence x(n) = [2, 1, +1, -2, 3, 5, 6, -7, 2, 0, 2, 1]. Use 8-point circular convolution in your approach using overlap add method. (08 Marks)
 - b. Solve for 8-point DFT of the sequence x(n) = [1, 1, 1, 1] using Radix 2 DIT-FFT algorithm. (08 Marks)
 - c. What is the speed improvement factor in calculating 128 point DFT of sequence using direct computation and FFT algorithm? (04 Marks)

Module-3

- 5 a. What are the different design techniques are available for FIR filter? Explain the four window techniques for the designing of FIR filter. (08 Marks)
 - b. A low pass filter is to be designed with the following desired frequency response.

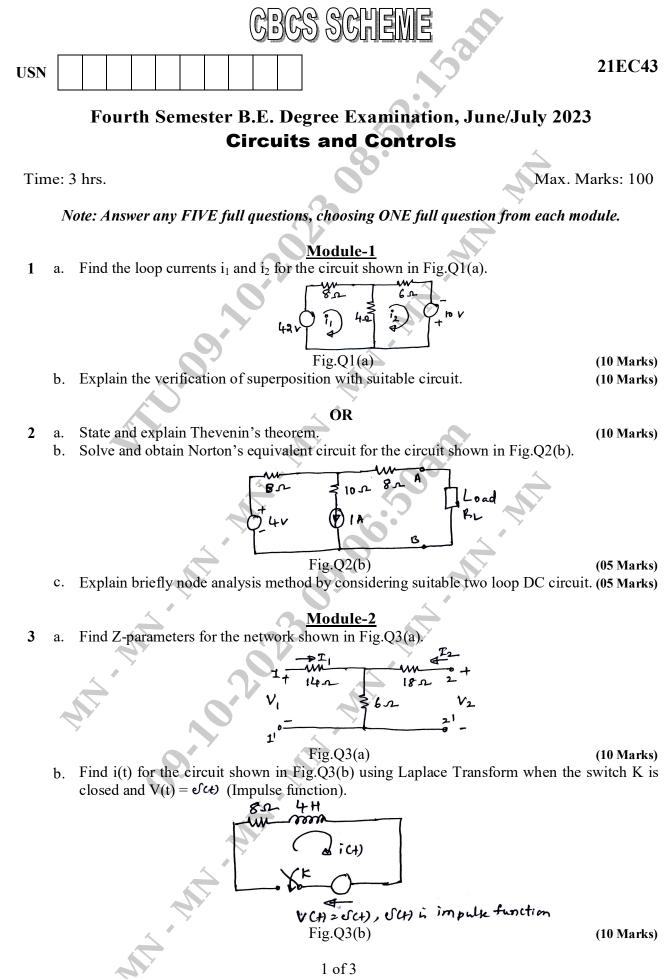
 $H_{d}(e^{f\omega}) = \begin{cases} e^{f^{3}\omega} & \text{for } |\omega| \le \frac{3\pi}{4} \\ 0 & \text{for otherwise} \end{cases}$

Determine $H(e^{f\omega})$ for M = 7 using Hamming window. (08 Marks) c Determine the direct form Relaization of the following :

$$h(n) = \delta(n) + \frac{1}{2}\delta(n-1) - \frac{1}{4}\delta(n-2) + \frac{1}{2}\delta(n-3).$$
 (04 Marks)

- a. Formulate the expression for symmetric FIR filter. 6 (08 Marks) b. Write a program and design for FIR Lowpass filter using humming window for M = 7 and $\omega_{c} = 3\pi/_{4} H_{d}(\omega) = \begin{cases} e^{-t3\omega} & \text{for } |\omega| \le \omega_{c} \\ 0 & \text{for otherwise} \end{cases}$ (08 Marks) c. Realize a linear phase FIR filter with following Impulse. Response H(z) = 1 + $\frac{3}{4}z^{-1} + \frac{17}{8}z^{-2} + \frac{3}{4}z^{-3} + z^{-4}$ in cascade form. (04 Marks) a. Given that $|H_a(\Omega)|^2 = \frac{1}{1+16\Omega^4}$. Determine the Analog filter system function $H_a(S)$. 7 (08 Marks) b. Develop an analog filter with maximally flat response. In pass band with acceptable, attenuation of 2dB at 20rad/sec, the alteration in stop band more than that 10dB beyond 30rad/sec. (08 Marks) c. Write program to implementation of IIR Butterworth Lowpass filter. (04 Marks) ØR Realization of direct form - I and direct form - II of IIR filter is given by 8 a. $H(z) = \frac{3+4z}{z-\frac{1}{2}} - \frac{2}{z-\frac{1}{4}}.$ (06 Marks) b. Make use of Bilinear transformation to obtain digital filter with $w_r = \frac{\pi}{2}$ and $\Omega = 4$ form given analog filter H_a(s) = $\frac{s+0.1}{(s+0.1)^2+16}$. (08 Marks) Write a program. Design and implementation of high pass filter to meet specification. c. (06 Marks) Module-5 Describe the IEEE single precision floating point digital signal processors. 9 a. (08 Marks) Describe the digital signal processes following units : b. i) Multiplier and accumulator ii) Address generation unit. (08 Marks) c. Determine following number into Q_{15} notation. i) 0560123 ii) -0.160123. (04 Marks) OR Explain fixed point digital signal processors of TMS320 family. 10 a. (08 Marks)
 - b. Explain digital signal processor using Harvard architecture. (06 Marks)
 c. Write a program for linear convolution of two sequences. Using DSK6713 DSP processor.

(06 Marks)



Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. 2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

4 a. Find Y-parameters for the network shown in Fig.Q4(a).

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b. State and explain Initial Value Theorem.

Module-3

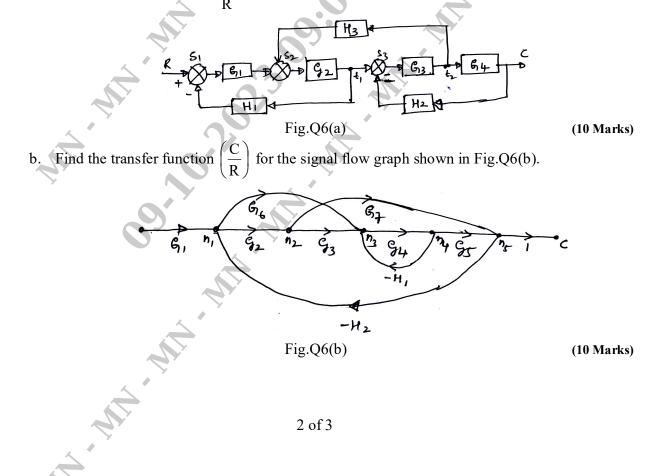
- 5 a. Explain the different types of control system.
 - b. Find the transfer function for the RLC circuit shown. Assume Initial condition as zero. RLC

circuit consists of voltage source of V_i as show in the Fig.Q5(b) and find $\frac{V_0(s)}{V_i(s)}$.

Fig.Q5(b)

OR

6 a. Find the transfer function $\frac{C}{R}$ for the block diagram as shown in Fig.Q6(a).



(10 Marks) (10 Marks)

(10 Marks)

(10 Marks)

<u>Module-4</u>

7 a. Find the output c(t) for the first order system, where

$$G(s) = \frac{a}{s+a}$$
 and $R(s) = \frac{1}{s}$ (10 Marks)

b. Explain the concept of stability and its stability necessary conditions. (10 Marks)

OR

- 8 a. Explain with a neat diagram of time response of second order system unit step function. Explain any five time specifications. (10 Marks)
 - b. Find the range of K for system stability. Given

Explain any four root locus plot rules.

9

a.

$$G(s) = \frac{K}{(s+2)(s+4)(s^2+6s+25)} \quad \text{and} \quad H(s) = 1.$$
 (10 Marks)

Module-5

RL

OR

(10 Marks)

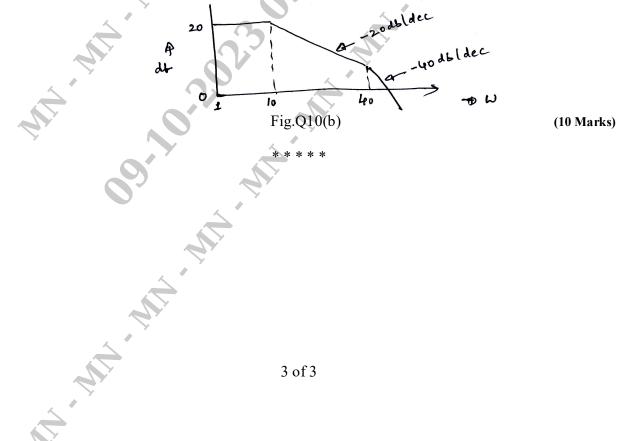
b. Find the state model of the given electrical system as shown in Fig.Q9(b).

Take state variables $X_1(t) = i(t)$ and $X_2(t) = V_0(t)$.

(10 Marks)

(10 Marks)

- 10 a. Find the state transition matrix for $A = \begin{bmatrix} 0 & -1 \\ 2 & -3 \end{bmatrix}$
 - b. Find the T. F (Transfer function) for the magnitude plot as shown in Fig.Q10(b).



Time: 3 hrs. Max. Marks: 100 Note: Answer any FIVE full questions, choosing ONE full question from each module. Module-1 Explain the time domain and frequency domain analysis of AM wave for a single 1 a. modulating signal with neat diagrams and necessary equations. (10 Marks) b. Explain the operation of envelope detector with neat diagrams and waveforms. Also mention the significance of RC-time constant. (05 Marks) c. An audio frequency signal $10\sin 2\pi(500)t$ is used to amplitude modulate a carrier of $50\sin 2\pi (10^5)$ t. Assume modulation index \Rightarrow 0.2. Determine sideband frequencies, amplitude of each side band, bandwidth required, Efficiency of AM wave. (05 Marks) OR With relevant diagrams, explain the operation of the quadrature carrier multiplexing 2 a. transmitter and receiver schemes. (07 Marks) Explain the concept of FDM with neat block diagram. b. (06 Marks) c. A carrier wave $4\sin(2\pi*500*10^3 t)$ volts is amplitude modulated by an audio wave $[0.2\sin 3(2\pi * 500t) + 0.1\sin 5(2\pi * 500t)]$ volts. Determine upper and lower sidebands and sketch the complete spectrum of the modulated wave. Estimate the total power in the sideband ($R = 1 \Omega$). (07 Marks) Module-2 3 Define the following : a. Instantaneous frequency (i) Maximum frequency deviation (ii) (iii) Modulation index. (06 Marks)

- Explain the generation of narrow band FM wave with neat block diagram, necessary b. equations and phasor diagrams. (08 Marks)
- c. When a 50.4 MHz carrier is frequency modulated by a sinusoidal AF modulating sinal, the highest frequency reached is 50.405 MHz. Calculate
 - The frequency deviation produced. (i)
 - Carrier swing of the wave. (ii)
 - Lowest frequency reached. (iii)

OR

- Explain the demodulation of FM signal using the nonlinear and linear model of PLL with a. neat diagrams and equations. (10 Marks)
 - Explain the FM stereo multiplexer and demultiplexer operation with neat diagrams. b.
 - (08 Marks) An FM wave is defined by $s(t) = 10\cos[2 + \sin 6\pi t]$. Find the instantaneous frequency of c. s(t). (02 Marks)

1 of 2

Fourth Semester B.E. Degree Examination, June/July 2023 **Communication Theory**

USN

CBCS SCHEME

21EC44

(06 Marks)

(06 Marks)

Module-3

- Write short notes on : 5 a
 - Thermal noise (i)
 - (ii) Shot noise.
 - (iii) White noise.
 - Derive the noise equivalent bandwidth equation $B = \frac{1}{4CR}$ Hz for low pass filter. (08 Marks) b.
 - Three 5 K Ω resistors are connected in series. For room temperature (KT = 4 × 10⁻²¹) and an C. effective noise bandwidth of 1 MHz, determine
 - The noise voltage appearing across each resistor. (i)
 - The noise voltage appearing across the series combination. (ii)
 - (iii) What is the rms noise voltage which appears across same three resistors connected in parallel under the same conditions? (06 Marks)

OR

Show the figure of merit for DSBSC system is unity. 6 а

- b. Obtain the expression for FOM of AM receivers using envelope detector. (08 Marks)
- An AM receiver operating with a sinusoidal wave of 80% modulation has an output signal to C. noise ratio of 30 dB. Calculate the corresponding channel S/N ratio. (04 Marks)

Module-4

What are the advantages of digitizing the analog sources? 7 (06 Marks) a. State and explain the sampling theorem for the band limited signal. Also explain the under b. sampling, over sampling and Nyquist rate with neat diagram. (14 Marks)

OR

8 Explain the pulse amplitude modulation with neat diagram and equations. a. (08 Marks) Explain the Time Division Multiplexing (TDM) with neat block diagram. b. (08 Marks)

An analog signal is expressed by the equation, $x(t) = \frac{1}{2}$ $-\cos(4000\pi t)\cos(1000\pi t)$. Calculate C. (04 Marks)

the nyquist rate and nyquist interval for this signal.

Module-5

- Explain the construction and regeneration of PCM signal. 9 (10 Marks) a.
 - Explain the different line codes. To transmit a bit sequence 01101001 draw the resulting b. waveforms using,
 - Unipolar NRZ (i)
 - Polar NRZ. (ii)
 - Unipolar RZ (iii)
 - (iv) **Bipolar** RZ
 - Manchester (v)

Write a short note on Vocoder.

c.

(10 Marks)

OR

Explain the concept and operation of delta modulation in detail. 10 a. (10 Marks) Explain quantization process with neat diagrams. Also explain the types of quantizer with b. neat diagrams.

(06 Marks) (04 Marks)

2 of 2

(08 Marks)