

MAHARAJA INSTITUTE OF TECHNOLOGY THANDAVAPURA

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VTU Question Papers

Electronics & Communication engineering-III,V & VII Semester

Feb/Mar-2022

2018 Scheme

Maharaja Institute of Technology Thandavapura

Just of NH-766, Mysore-Ooty highway, Thandavapura(Vill & Post), Nanjangud Taluk, Mysore District-571302.

INDEX

Sl No.	Subject Code	Subject Title	Exam Date	
1	18MAT31	TRANSFORM CALCULUS, FOURIER	FEB/MAR-2022	
		SERIES AND NUMERICAL		
		TECHNIQUES		
2	18MATDIP31	ADDITIONAL MATHEMATICS-I	FEB/MAR-2022	
3	1ECE32	NETWORK THEORY	FEB/MAR-2022	
4	18EC33	ELECTRONIC DEVICES	FEB/MAR-2022	
5	18EC34	DIGITAL SYSTEM DESIGN	FEB/MAR-2022	
6	18EC35	COMPUTER ORGANIZATION AND	FEB/MAR-2022	
		ARCHITECTURE		
7	18EC36	POWER ELECTRONICS AND	FEB/MAR-2022	
		INSTRUMENTATION		
8	18ES51	TECHNOLOGICAL INNOVATION	FEB/MAR-2022	
		MANAGEMENT AND		
		ENTREPRENEURSHIP		
9	18EC52	DIGITAL SIGNAL PROCESSING	FEB/MAR-2022	
10	18EC53	PRINCIPLES OF COMMUNICATION	FEB/MAR-2022	
		SYSTEMS		
11	18EC54	INFORMATION THEORY AND	FEB/MAR-2022	
		CODING		
12	18EC55	ELECTROMAGNETIC WAVES	FEB/MAR-2022	
13	18EC56	VERILOG HDL	FEB/MAR-2022	
14	18EC71	COMPUTER NETWORKS	FEB/MAR-2022	
15	18EC72	VLSI DESIGN	FEB/MAR-2022	
16	18EC731	REAL TIME SYSTEMS	FEB/MAR-2022	
17	18EC744	CRYPTOGRAPHY	FEB/MAR-2022	

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Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. 2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

18MAT31

c. Obtain the Fourier expansion of y upto the first harmonic given :

9

y

0 2 3 4 5 х

18

(07 Marks)

20

Module-

24

28

26

5	a.	If $f(x) = \begin{cases} 1, & x < a \\ 0, & x > a \end{cases}$, find the Fourier transform of $f(x)$ and hence	e find the
		value of $\int_{0}^{\infty} \frac{\sin x}{x} dx$	(06 Marks)
	b.	Find the infinite Fourier cosine transform of $e^{-\alpha x}$.	(07 Marks)
	c.	Solve using z-transform $y_{n+2} - 4y_n = 0$ given that $y_0 = 0$, $y_1 = 2$	(07 Marks)
		OR	``´´
6	a.	Find the fourier sine transform of $f(x) = e^{- x }$ and	
		hence evaluate $\int_{0}^{\infty} \frac{x \sin mx}{1+x^2} dx$; $m > 0$.	(06 Marks)
	b.	Obtain the z-transform of $\cos n\theta$ and $\sin n\theta$.	(07 Marks)
	c.	Find the inverse z-transform of	· · · ·
		$\frac{4z^2 - 2z}{z^3 - 5z^2 + 8z - 4}$	(07 Marks)
		Module-4	
7	a.	Solve $\frac{dy}{dx} = x^3 + y$, $y(1) = 1$ using Taylor's series method considering up to four	rth degree
		terms and find y(1.1).	(06 Marks)
		dy v	

- b. Given $\frac{dy}{dx} = 3x + \frac{y}{2}$, y(0) = 1 compute y(0.2) by taking h = 0.2 using Runge Kutta method of fourth order. c. If $\frac{dy}{dx} = 2e^x y$, y(0) = 2, y(0.1) = 2.010, y(0.2) = 2.040 and y(0.3) = 2.090, find y(0.4)
- correct to 4 decimal places using Adams-Bashforth method. (07 Marks)

OR

- Use fourth order Runge-Kutta method, to find y(0.8) with h = 0.4, given $\frac{dy}{dx} = \sqrt{x+y}$, 8 a. y(0.4) = 0.41(06 Marks)
 - b. Use modified Euler's method to compute y(20.2) and y(20.4) given that $\frac{dy}{dx} = \log_{10}\left(\frac{x}{y}\right)$ with y(20) = 5 Taking h = 0.2, (07 Marks)

c. Apply Milne's predictor-corrector formulae to compute y(2.0) given $\frac{dy}{dx} = \frac{x+y}{2}$ with

				G 21	-
X	0.0	0.5	1.0	1.5	
у	2.000	2.6360	3.5950	4.9680	

(07 Marks)

18MAT31

<u>Module-5</u>

- a. Using Runge-Kutta method, solve 9 $\frac{d^2y}{dx^2} = x \left(\frac{dy}{dx}\right)^2 - y^2$, for x = 0.2, correct to four decimal places, using initial conditions y(0) = 1, y'(0) = 0(07 Marks)
 - b. Derive Euler's equation in the standard form viz, $\frac{\partial f}{\partial y} \frac{d}{dx} \left(\frac{\partial f}{\partial y'} \right) = 0$ (07 Marks)
 - c. Find the extremal of the functional $\int_{x_1}^{x_2} (y^2 + y'^2 + 2ye^x) dx$

(06 Marks)

OR

Given the differential equation $2\frac{d^2y}{dx^2} = 4x + \frac{dy}{dx}$ and the following table of initial values: 10 a.

		(dx^2	dx X		
	Х	1	1.1	1.2	1.3	
5	у	2	2.2156	2.4649	2.7514	
Ŧ	y'	2	2.3178	2.6725	2.0657	

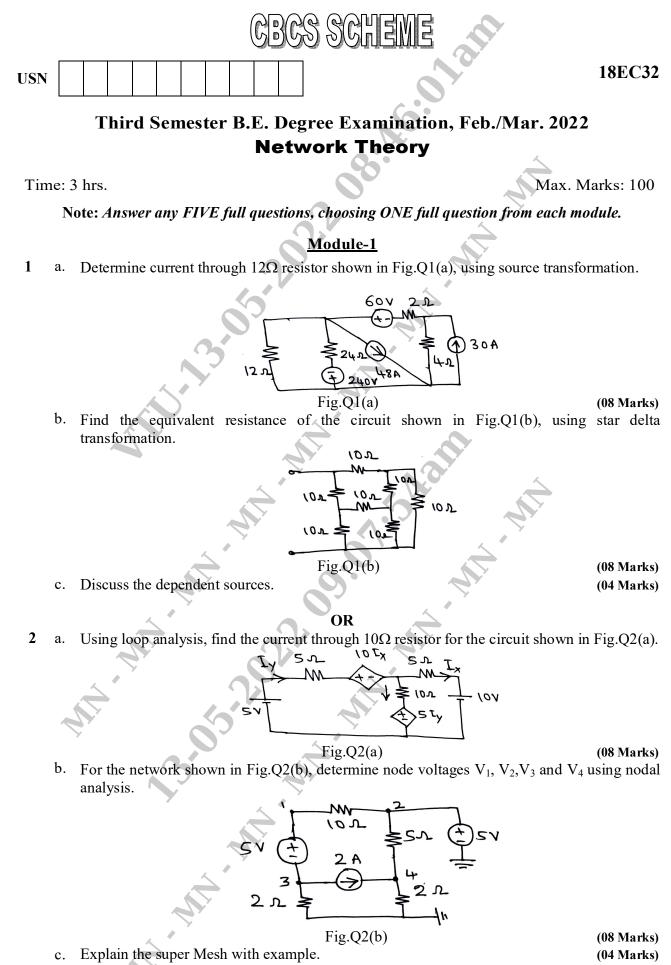
	Compute y(1.4) by applying Milne's Predictor-corrector formula.	(07 Marks)
b.	Prove that geodesics of a plane surface are straight lines.	(07 Marks)

On what curves can the functional $\int_{0}^{1} (y'^{2}+12xy)dx$ with y(0) = 0, y(1) = 1 can be c. Stratic Mit - Mit extremized? (06 Marks)

3 of 3

M

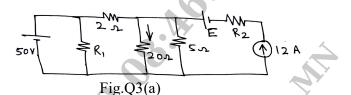
			18MATDIP31
(0	OR	
6	a.	Find the directional derivate of $\phi = x^2yz + 4xz^2$ at (1,-2,-1) along $\vec{a} = 2\hat{i} - \hat{j}$	
	b.	Find curl \vec{f} given that $\vec{f} = xyz^2 \hat{i} + xy^2 z \hat{j} + x^2 yz \hat{k}$.	(06 Marks)
	c.	If $\vec{f} = x^2i + y^2j + z^2k$ and $\vec{g} = yzi + zxj + xyk$. Show that $\vec{f} \times \vec{g}$ is a solenoid <u>Module-4</u>	lal vector. (07 Marks)
7	a.	Obtain the reduction formula, $I_n = \int \overline{\cos^n x dx}$, where n is a positive integer.	(07 Marks)
	b.	Evaluate $\int_{0}^{1} \int_{x}^{\sqrt{x}} xy dy dx$.	(06 Marks)
	c.	Evaluate $\int \int \int (x + y + z) dx dy dz$.	(07 Marks)
0	_	0 0 0 0 π/6 OR	
8	a.	Evaluate : $\int_{0} \sin^{6}(3x) dx$.	(07 Marks)
	b.	Evaluate : $\int_{0}^{\pi} x \sin^{4} x \cos^{6} x dx$	(06 Marks)
	c.	Evaluate $\iint_{0} \iint_{0} \int_{0} \int_{0} xyz dx dy dz$.	(07 Marks)
9	a.		(07 Marks)
2	b.	Solve : $(4xy + 3y^2 - x) dx + (x^2 + 2xy) dy = 0.$	(06 Marks)
	c.	Solve : $y(2xy + e^{-}) dx - e^{-} dy = 0$.	(07 Marks)
		OR	
10		Solve : $(5x^2 + 3x^2y^2 - 2xy^2)dx + (2x^3y - 3x^2y^2 - 5y^2)dy = 0.$ Solve : $y(2xy + 1)dx - x dy = 0.$	
	c.		
		dx	× ,
		2 of 2	
9	с. а. b.	Solve : $y(2xy + e^x) dx - e^x dy = 0$. Solve : $(5x^4 + 3x^2y^2 + 2xy^3)dx + (2x^3y - 3x^2y^2 - 5y^4)dy = 0$. Solve : $y(2xy + 1)dx - x dy = 0$. Solve : $\frac{dy}{dx} + y \cot x = \cos x$. *****	(07 Marks (06 Marks (07 Marks (06 Marks (07 Marks)



1 of 4

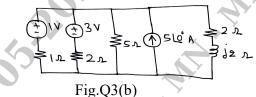
Module-2

3 a. Using super position theorem, find the current through 20Ω resistor shown in Fig.Q3(a).



(08 Marks)

b. Using Millman's theorem, determine the current through $(2 + j2)\Omega$ impedance for the network shown in Fig.Q3(b).

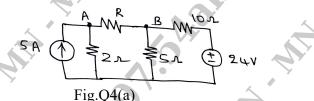


(08 Marks)

c. State the Norton's theorem and also write the procedure to be followed for solving the problem. (04 Marks)

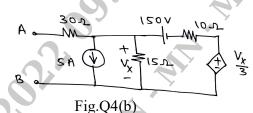
OR

4 a. What should be the value of R such that maximum power transfer can takes place from the rest of the network to R. Obtain the amount of this power for circuit shown in Fig.Q4(a).



(08 Marks)

b. Obtain the Thevinin's equivalent circuit cross AB for the circuit shown in Fig.Q4(b).

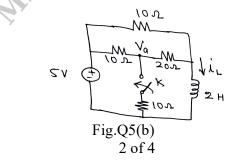


(08 Marks)

c. State the maximum power transfer theorem and also write equation of P_{max} for both DC and AC circuits. (04 Marks)

Module-3

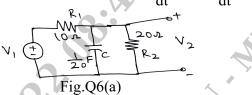
- 5 a. Explain the transient behavior of the resistance, inductance and capacitor. Also write the procedure for evaluating transient behavior. (10 Marks)
 - b. In the network shown in Fig.Q5(b), a steady state is reached with the swatch 'K' open. At t = 0 the switch is closed. Determine the value of $V_a(0^+)$ and $V_a(0^-)$.



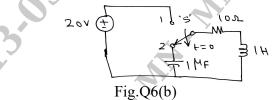
(10 Marks)

OR

6 a. For the network shown in Fig.Q6(a) $V_1(t) = e^{-t}$ for $t \ge 0$ and is zero for all t < 0. If the capacitor is initially uncharged determine the value of $\frac{d^2v_2}{dt^2}$ and $\frac{d^3v_2}{dt^3}$ at $t = 0^+$.



b. The switch 'S' is changed from position 1 to position 2 at t = 0. Steady state conditions have been reached in position 1. Find the value of i, $\frac{di}{dt}$ and $\frac{d^2i}{dt^2}$ at $t = 0^+$ for the circuit shown in Fig.Q6(b).



(10 Marks)

(10 Marks)

<u>Module-4</u>

f(t)

7 a. Find the Laplace transform of f(t) shown in Fig.Q7(a).

(10 Marks)

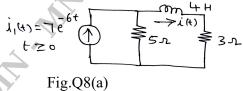
Fig.Q7(a) b. Find the Lapalce transform of the pulse shown in Fig.Q7(b).

(10 Marks)

OR

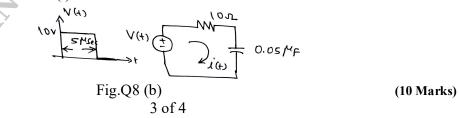
Fig.Q7(b)

8 a. Find i(t) for the circuit shown in Fig.Q8(a).



(10 Marks)

b. A voltage pulse of 10V and 5µsec duration is applied to the RC network shown in Fig.Q8(b). Find the current i(t).



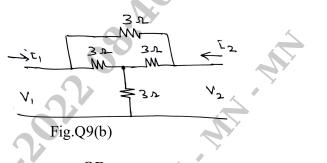
<u>Module-5</u>

Obtain y-parameters interms of z-parameters and h-parameters. 9 a. b.

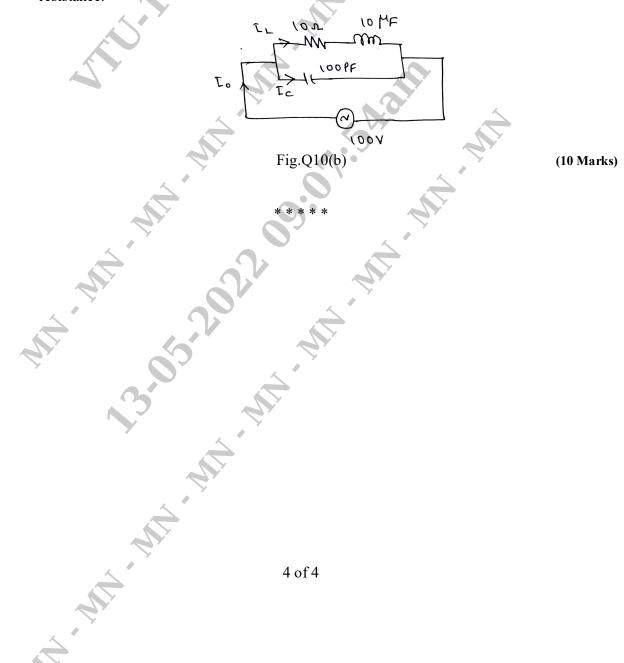
10 a. For the network shown in Fig.Q9(b), find the T-parameters.

(10 Marks)

(10 Marks)



- OR Derive the expression of bandwidth, half power frequencies and selectivity of a series
- resonance circuit. (10 Marks) b. For the parallel resonant circuit shown in Fig.Q10(b), find I₀, I_L, I_C, f₀ and dynamic resistance.



2

18EC33

Third Semester B.E. Degree Examination, Feb./Mar. 2022 Electronic Devices

GBGS SGHEME

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Explain classification of semiconductor insulator and metals using energy band diagram.
 - b. Explain different types of bonding forces in solids.
 - c. What are intrinsic and extrinsic materials? Explain briefly by taking suitable example.

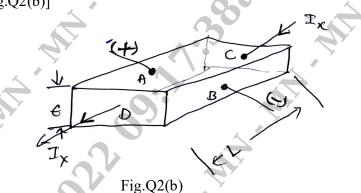
(08 Marks)

(08 Marks)

(04 Marks)

OR

- a. Define Hall effect in semiconductor. Obtain an expression for mobility interms of Hall coefficient and resistivity. (08 Marks)
 - b. Consider a semiconductor bar with width w = 0.1 mm, thickness $t = 10 \mu m$, length L = 5 mm. For B = 10 KG (1 KG = 10^{-5} wb/cm²) and current of 1 mA. We have $V_{AB} = -2mV$ and $V_{CD} = 100$ mV. Find the type, concentration and mobility of the majority carrier. [Refer Fig.Q2(b)]



(04 Marks)

c. Derive an expression for conductivity and mobility from random thermal motion or electron in solid. (08 Marks)

Module-2

- 3 a. Explain the reverse bias p-n junction indicating the minority carrier distribution and variation of quasi fermi levels. (10 Marks)
 - b. With a neat diagram, explain in detail Avalanche Breakdown and derive an approximate analysis of avalanche multiplication. (10 Marks)

OR

- 4 a. Derive an expression for current and voltage for an illuminated junction of protodiode and discuss the operation in various quadrants in I-V characteristic. (08 Marks)
 - b. Explain the structure and operation of solar cell. Indicate the significance of Fill Factor.

(08 Marks)

c. A solar cell has a short circuit current of 100 mA and open circuit voltage of 0.8 V under full solar illumination fill factor is 0.7. What is maximum power delivered to load by this cell?

Module-3

- 5 a. Explain the summary of hole flow and electron flow in p-n-p transistor with proper biasing and list three dominant mechanism which accounts for I_B . (10 Marks)
 - b. Explain the process flow for double polysilicon self aligned BJT Fabrication. (10 Marks)

OR

6 a. Derive Eber's moll modes for Assymetric Transistor (coupled diode model). (10 Marks)
b. Write short notes on: (i) Base narrowing (ii) Avalanche Breakdown in transistor (10 Marks)

<u>Module-4</u>

- 7 a. Explain the structure and operation of pn JFET by varying V_{GS} and VDS independently.
 - b. Write the small signal equivalent circuit of JFET and obtain the expression for transconductance (gm) and plot the graph with respect to V_{gs} . (06 Marks)
 - c. Explain the operation of MOS capacitor using energy band diagram for p-type substrate when:
 - (i) Negative gate bias
 - (ii) Moderate positive gate bias
 - (iii) Large positive gate bias

(08 Marks)

(05 Marks)

(05 Marks)

(05 Marks)

(05 Marks)

(06 Marks)

OR

- 8 a. Explain the ideal capacitance voltage characteristics of an MOS capacitor with p-type substrate. (08 Marks)
 - b. Explain the operation of n-channel enhancement MOSFET and obtain the current voltage relationship. (08 Marks)
 - c. Write the different types of MOS structures and symbols for each. (04 Marks)

Module-5

- 9 Explain briefly the various steps involved in the fabrication of p-n junction:
 - a. Rapid thermal processing
 - b. Ion implementation
 - c. Chemical Vapor Deposition (CVD)
 - d. Photolithography

OR _

10a. Write a note on Integrated Circuit (IC) and its advantages and types of ICs.(10 Marks)b. Explain the fabrication of CMOS twin well process.(10 Marks)

USN			18EC34							
		Third Semester B.E. Degree Examination, Feb./Mar. 202	2							
		Digital System Design	4							
Tin	ne: 3	3 hrs.	Marks: 100							
	N	lote: Answer any FIVE full questions, choosing ONE full question from each m	odule.							
1	a.	Define and explain the combinational logic circuit along with block diagram.	(06 Marks							
1		Develop the canonical minterm and maxterm forms in decimal notation for t								
		Boolean functions:								
		i) $X = f(a, b, c, d) = \overline{ab} + c\overline{d}$								
		ii) $Y = f(a, b, c) = (\bar{a} + b)(b + \bar{c})$	(08 Marks							
	c.	Simplify the following function using K-map method and also construct logic c simplified equation (function).	ircuit for th							
		$Y = f(a, b, c, d) = \sum(0, 1, 2, 4, 5, 6, 8, 9, 10, 12, 13, 14).$	(06 Marks							
			× ·							
2		Cimulify the following Declean function by using O. Marsthadi								
Z	a.	Simplify the following Boolean function by using Q-M method: $X = f(a, b, c) = \sum (0, 1, 2, 3, 4, 5, 6).$	(10 Marks							
	b.	Design a combinational logic circuit for valid single digit BCD data, the output is								
	_	1 whenever a number is greater than 5 appears at the input.	(05 Marks							
	c.	Identify the PI and EPI for the following function: $M = f(a, b, c, d) = \sum (1, 2, 3, 5, 7, 11, 12, 13, 14, 15).$	(05 Marks							
		M I(d, 0, 0, d) Z(1, 2, 3, 5, 7, 11, 12, 13, 14, 15).								
-		Module-2								
3	a. b.	Draw and explain the circuit for 3 to 8 decoder. Design and implement a full adder circuit using logic gates.	(06 Marks (08 Marks							
	с.	Write a short notes on PLD's and FPGA.	(06 Marks							
4	a.	OR Define MUX and explain 4:1 MUX with the help of logic diagram using gates.	(06 Marks							
т		Explain 4-bit carry look-ahead adder with diagram.	(08 Marks							
		Design and implement 1-bit comparator circuit.	(06 Marks							
		Module-3								
5	a.	Compare sequential circuit and combinational circuits.	(06 Marks							
	b.	Write a short notes on SR-latch.	(06 Marks							
	c.	Illustrate master-slave J-K flip-flop using NAND Gates.	(08 Marks							
		OR								
6	a.	Distinguish between synchronous and asynchronous counter.	(06 Marks							
	b. с.	Explain 4-bit universal shift register along with diagram. Explain the working of clocked SR-FF using NAND Gates.	(08 Marks (06 Marks							
	C.	Explain the working of clocked SR-11 using NAND Gates.	(00 WIAI KS							
		1 of 2								

CBCS SCHEME

(10 Marks)

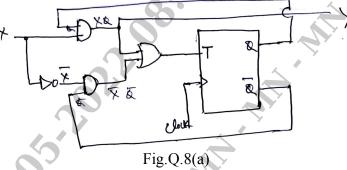
(10 Marks)

Module-4

- 7 Explain Mealy and Moore model with diagrams. a.
 - Design and develop Mod-6 synchronous counter using T-FF b.

OR

Construct the excitation table, transition table, state table and state diagram for the following 8 a. sequential circuit. (Refer Fig.Q.8(a)). (14 Marks)



List out the applications of shift registers along with brief explanation. b.

(06 Marks)

Module-5

9 Explain the operation of serial adder with accumulator. a. (12 Marks) Illustrate state assignment rules. b. (08 Marks)

OR

- Write a short notes on: 10 a.
 - Sequential circuit design steps i)
 - BCD to Ex-3 code convertor. ii)
 - Explain 4-bit Ring and Johnson counter along with diagram. b.

(10 Marks) (10 Marks)

2 of 2

USN

1

18EC35

(04 Marks)

(04 Marks)

(04 Marks)

Third Semester B.E. Degree Examination, Feb./Mar. 2022 Computer Organization and Architecture

GBCS SCHEME

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- a. Explain the basic operational concept between the processor and memory with neat block diagram. (08 Marks)
 - b. Explain the various parameters affecting the performance of a computer and also provide the basic performance equation. (08 Marks)
 - c. Write a short note on single bus structure with neat diagram.

OR

- 2 a. List out and explain the three systems used for representing signed numbers and also brief about the modular number system concept. (08 Marks)
 - b. Explain IEEE standard used for single and double precession floating point number representation with examples. (08 Marks)
 - c. Write a short note on Big-endian and little-endian assignment.

Module-2

- 3 a. What is addressing mode? Explain any four addressing modes with examples. (08 Marks)
 b. What are assembler directives? Explain about the various directives used in the program with example. (08 Marks)
 - c. Write a short note on the assembly and execution of programs. (04 Marks)

OR

- 4 a. With neat diagram and program example, explain a simple I/O task between processor, keyboard and display. (10 Marks)
 - b. What is subroutine? Illustrate the subroutine function with parameter passing by value and reference with suitable program. (10 Marks)

<u>Module-3</u>

- a. Explain the concept of memory mapped I/O with neat diagram of I/O interface with program example. (10 Marks)
- b. Write short notes on: (i) Interrupt hardware (ii) Interrupt nesting (10 Marks)

OR

- 6 a. What is an interrupt? Explain about various implementation techniques of interrupt.
 - b. Explain how simultaneous interrupt request is handled using the concept of Daisy Chain. (10 Marks)

Module-4

- 7 a. Explain the internal organization of memory chips with example. (08 Marks)
 - b. Explain the internal organization of $2M \times 8$ DRAM chip with neat diagram. (08 Marks)
 - c. Write a short note on ROM.

5

OR

- 8 a. Discuss about the use of cache memory in the processor system.
 - b. What is virtual memory? Explain its organization with neat diagram.
 - c. Write a short note on magnetic hard disk.

Module-5

- 9 a. Explain single-bus organization of the data path inside a processor with neat diagram.
 - b. Explain the process of fetching a data word from memory using respective registers of a processor with neat diagram. (10 Marks)

OR

- 10 a. Explain the control signal generation required for proper sequence of instructions in the processor. (10 Marks)
 - b. What is microprogrammed control? Explain its basic organization with suitable diagram and example. (10 Marks)

(04 Marks)



USN

1

18EC36

Third Semester B.E. Degree Examination, Feb./Mar. 2022 Power Electronics and Instrumentation

Time: 3 hrs.

Max. Marks: 100

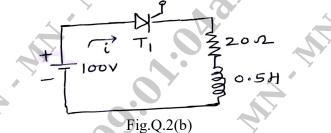
Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- a. Mention the different types of power electronic converters. Explain the significance, functions and applications of them. (07 Marks)
 - b. Explain the static Anode-Cathode characteristics of SCR with circuit diagram and V-I characteristics. (08 Marks)
 - c. Explain the basic operation of the unijunction transistor with basic UJT structure, UJT symbol and equivalent circuit. (05 Marks)

OR

- 2 a. Mention the applications of power electronics in various sectors. (07 Marks)
 - b. The latching current of a thyristor circuit is 50mA. The duration of the firing pulse is 50µs. Will the thyristor get fired? (05 Marks)



 c. Explain the operation of the resistance firing circuit with associated voltage waveforms. Derive the relevant expressions.
 (08 Marks)

<u>Module-2</u>

- 3 a. Explain the operation of the single phase half wave controlled rectifier with resistive load using circuit and waveforms. (10 Marks)
 - b. Give basic chopper classification with different chopper configurations. (05 Marks)
 - c. A dc chopper circuit connected to a 100V dc source supplies an inductive load having 40mH in series with a resistance of 5 Ω . A freewheeling diode is placed across the load. The load current varies between the limits of 10A and 12A. Determine the time ratio of the chopper. (05 Marks)

OR

- 4 a. Explain the effect of freewheeling diode with half wave controlled rectifier circuit and waveforms using inductive load. (10 Marks)
 - b. Explain the operation of step-up/down choppers with suitable circuit. Derive the relevant expression. (07 Marks)
 - c. A step-up chopper is used to deliver load voltage of 500V from a 220V dc source. If the blocking period of the thyristor is 80µs. Compute the required pulse-width. (03 Marks)

(07 Marks)

(07 Marks)

Module-3

- 5 a. Explain the operation of the single phase half bridge inverter with RL load. Draw the relevant circuit and waveforms. (10 Marks)
 - b. Explain the operation of the isolated forward converter with suitable circuit diagram and relevant waveforms. Mention the advantages and disadvantages. (10 Marks)

OR

- 6 a. Explain the types of errors in measurements.
 - b. Explain the operation of the multirange voltmeter with normal circuit and with multipliers connected in series string circuit. (07 Marks)
 - c. A 1mA meter movement having an internal resistance of 100Ω is used to convert into a multirange ammeter having the range 0-10mA, 0-20mA, and 0-30mA. Determine the value of the shunt resistance required.
 (06 Marks)

Module-4

- 7 a. Explain the operation of dual slope integrating type DVM with basic principles and suitable block-diagram. (08 Marks)
 - b. With suitable block diagram, explain the operation of measurement of time briefly.
 - c. A capacitance comparison bridge is used to measure a capacitive impedance at a frequency of 2kHz. This bridge constants at balance are $c_3 = 100\mu$ F, $R_1 = 10K\Omega$, $R_2 = 50K\Omega$, $R_3 = 100K\Omega$. Find the equivalent series circuit of the unknown capacitance. (05 Marks)

OR

- 8 a. With suitable block diagram and table explain the operation of successive approximation DVM. (08 Marks)
 - b. With suitable block diagram approach explain the operation of the digital frequency meter. (07 Marks)
 - c. Find the equivalent parallel resistance and capacitance that causes a Wien bridge to null with the following component values $R_1 = 3.1K\Omega$, $C_1 = 5.2\mu$ F, $R_2 = 25K\Omega$, f = 2.5kHz, $R_4 = 100$ K Ω . (05 Marks)

Module-5

- 9 a. Explain the operation of the resistive position transducer with construction and electrical equivalent circuit. (07 Marks)
 - b. In the differential instrumentation amplifier using transducer bridge, $R_1 = 2.2K$, $R_F = 10K$, $R_A = R_B = R_C = 120K$, E = +5V and op-amp supply voltage $= \pm 15V$, the transducer is a transistor with the following specifications. $R_T = 120K$ at a reference temperature of 25°C. Temperature coefficient of resistance = $-1K/^{\circ}C$. Determine the output voltage at 0°C and $100^{\circ}C$. (06 Marks)
 - c. Explain the PLC structure with block diagram. And also explain the PLC operation with PLC operation diagram. (07 Marks)

OR

- 10 a. Explain the operation of the LVDT with construction, various core positions of it, and variation of output voltage vss displacement. (10 Marks)
 - b. What is the significance of analog weight scale? Using strain gauge bridge circuit for analog weight scale explain its operation briefly. (05 Marks)
 - c. With Bell circuit diagram, explain the operation of the Programmable Logic Controller (PLC) relays. (05 Marks)

					G	BCC	S SCHE	MB		
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	L	Fifth	Seme	ster	B.E. 1	Degi	ee Examin	ation, Fe	b./Mar. 202	2
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					En	tre	preneurs	hip		
Tin	ne: 3	3 hrs.					8.		Max. N	Aarks: 100
	Ν	ote: Answei	r any F	IVE f	ull que	stions	, choosing ON	E full quest	ion from each n	nodule.
1	a.	Define Ma	nageme	ent. Ex	xplain a	ny fo	Module-1 ur Managemen	t functions.		(10 Marks)
	b.	Explain rol	les of a	Mana	ger.					(10 Marks)
2	a.	Define Plan	nning. I	Explai	n any fo	our lii	OR mitations of Pla	anning.		(10 Marks)
	b.	Explain typ	bes of E	Decisio	on maki	ng.				(10 Marks)
3	a.	Define Org	vanisatio	on Ex	nlain th		Module-2 nciples of Orga	nizino		(10 Marks)
U	b.						os involved in S		cess.	(10 Marks)
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	b.	Discuss an	y five p	urpos	e of Co	mmu	nication in an (Organization	\sim	(10 Marks)
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U	a.			•			3			(10 Marks)
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7	a.	Explain in	brief, tl	ne cha	racteris		<u>Module-4</u> f Family owne	d business in	India.	(10 Marks)
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	b. c.	Explain M What is Ec								(10 Marks) (02 Marks)
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9	a. b.				N		asons for prepa es for funding	-	ess Plan.	(10 Marks) (10 Marks)
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10	a.							rtance of Net	twork Analysis.	
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Fifth Semester B.E. Degree Examination, Feb./Mar.2022 **Digital Signal Processing** Time: 3 hrs. Max. Marks: 100 Note: Answer any FIVE full questions, choosing ONE full question from each module. Module-1 a. Prove that the sampling of DTFT of a sequence x(n) result in N-point DFT with a neat diagram. b. Find the 4-point DFT of the sequence $x(n) = \{1, 0, 0, 1\}$ using matrix method and verify the answer by taking the 4-point IDFT of the result. OR Derive the circular Time shift property. Compute the circular convolution of the following sequences using DFT and IDFT method

GBGS SGHEME

W(n) = $\frac{1}{2} + \frac{1}{2} \cos \left[\frac{2\pi}{N} \left(n - \frac{N}{2} \right) \right]$, what is the DFT of the window sequence c.

y(n) = x(n).w(n)? Relate the answer in terms of X(K)

Module-2

- Find the output y(n) of a filter whose impulse response is $h(n) = \{1, 1, 1\}$ and the input 3 a. signal $x(n) = \{3, -1, 0, 1, 3, 2, 0, 1, 2, 1\}$ using overlap-add method. Assume the length of each block N is 6. (10 Marks)
 - What do you mean by computational complexity? Compare the direct computation and FFT algorithms. In the direct computation of 32-point DFT of x(n), How many
 - **Complex** multiplications (i)

 $x_1(n) = \{1, 2, 3, 4\}$ and $x_2(n) = \{4, 3, 2, 1\}$.

- (ii) Complex additions.
- Real multiplications. (iii)
- (iv) Real additions and
- Trigonometric function evaluations are required. v)

OR

Develop 8-point DIT-FFT Radix-2 algorithm and draw the signal flow graph. 4 a. (10 Marks) Given x(n) = n+1 for $0 \le n \le 7$. Find X(K) using DIF-FFT algorithm. b. (10 Marks)

Module-3

What are the different design techniques available for the FIR filters? Explain Gibbs 5 a. phenomenon. Explain the four window techniques for the designing of FIR filters.

(10 Marks)

(10 Marks)

b. A low pass filter is to be designed with the following desired frequency response,

$$H_{d}(e^{J\omega}) = \begin{cases} e^{-J3\omega} , \text{ for } -\frac{3\pi}{4} \le \omega \le \frac{3\pi}{4} \\ 0 , \frac{3\pi}{4} \le \omega \le \pi \end{cases}$$

Determine $H(e^{J\omega})$ for M = 7 using Hamming window.

(10 Marks)

18EC52

(10 Marks)

(10 Marks)

(06 Marks)

(09 Marks)

(05 Marks)

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1

2

a.

b.

(10 Marks)

6 a. A FIR filter is given by,

$$y(n) = x(n) + \frac{2}{5}x(n-1) + \frac{3}{4}x(n-2) + \frac{1}{3}x(n-3)$$

Draw the lattice structure.

b. Based on the frequency-sampling method, determine the coefficients of a linear-phase FIR filter of length M = 15 which has a symmetric unit sample response and a frequency response that satisfies the conditions.

$$H\left(\frac{2\pi}{15}K\right) = 1; \qquad K = 0, 1, 2, 3$$
$$= 0.4; \qquad K = 4$$
$$= 0 \qquad ; \qquad K = 5, 6, 7$$

(10 Marks)

Module-4

The normalized transfer function of a 2^{nd} order Butterworth filter is given by, 7 a.

$$H_2(S) = \frac{1}{S^2 + 1.414S + 1}$$

Convert the analog filter into digital filter with cut-off frequency of 0.5π rad/sec using bilinear transformation. Assume T = 1 sec. (10 Marks)

b. A filter is given by the difference equation $y(n) - \frac{1}{4}y(n-1) + \frac{1}{8}y(n-2) = x(n) + \frac{1}{2}x(n-2)$.

Draw direct form - I and direct form - II realizations. Also obtain the transfer function of the filter. (10 Marks)

OR

- Derive mapping function used in transforming analog filter to digital filter by bilinear 8 a. transformation, preserves the frequency selectivity and stability properties of analog filter.
 - b. Design an IIR digital Butterworth filter that when used in the analog to digital with digital to analog will satisfy the following equivalent specification.
 - Low pass filter with -1 dB cut off 100 π rad/sec. (i)
 - Stop band attenuation of 35 dB at 1000 π rad/sec. (ii)
 - (iii) Monotonic in stop band and pass band.
 - Sampling rate of 2000 rad/sec. (iv)
 - Use bilinear transformation. (v)

(10 Marks)

(10 Marks)

Module-5

- 9 With the block diagram, explain Digital Signal processors based on the Harvard architecture.
 - b. Discuss briefly the following special digital signal processor hardware units:
 - Multiplier and Accumulator (MAC) unit. (i)
 - (ii) Shifters.
 - (iii) Address Generators.

OR

- Discuss the following IEE Floating-point formats: 10 a.
 - Single precision format. (i)
 - (ii) Double precision format.
 - With the diagram, explain the basic architecture of TMS320C54X family processor. b.

(10 Marks)

(10 Marks)

* * * * 2 of 2

(10 Marks)

(10 Marks)



Fifth Semester B.E. Degree Examination, Feb./Mar. 2022 **Principles of Communication Systems**

Time: 3 hrs.

b.

1

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- Write an AM wave expression in time domain and in frequency domain. Draw AM a. waveform. (07 Marks)
 - With neat diagram, explain the demodulation of AM wave using envelope detector. b.

(08 Marks)

c. An audio frequency signal $M(t) = 5 \sin 2\pi (10^3)t$ is used to amplitude modulate a carrier of $C(t) = 100 \sin 2\pi (10^6)t$. Assume modulation index $\mu = 0.4$. Find: i) Sideband frequencies ii) Amplitude of each sideband iii) Bandwidth iv) Total power delivered to a load of v) Find efficiency of AM wave, assume $R = 1\Omega$. 100u (05 Marks)

OR

- Explain the generation of DSBSC wave using a Ring modulator. 2 a. (10 Marks)
 - Explain with a neat diagram, the working of Quadrature Carrier Multiplexing (QAM).

(08 Marks)

(07 Marks)

An AM signal with a carrier of 1kW has 200W in each sideband. What is the percentage of c. modulation? (02 Marks)

Module

- Define angle modulation. Derive the FM wave expression in time domain. 3 a. (08 Marks) Define the following terms: b.
 - Modulation index i)
 - Frequency deviation ii)
 - Bandwidth iii)
 - A FM wave is represented by the equation $V = 10 \sin [5 \times 10^8 t + 4 \sin 1250 t]$. C. Find: i) Carrier frequency and modulating frequency ii) Modulation index and frequency iii) Bandwidth using Carson's rule. deviation (05 Marks)

OR

Write the basic block diagram of PLL. Derive the expression for non-linear model of PLL. 4 a (10 Marks)

- Explain the direct method of generating FM wave using Hartley oscillator with relevant b. equations and diagram. (06 Marks) (04 Marks)
- Write the Narrowband FM and wideband FM expression. C.

Module-3

- Derive the expression for figure of merit of an AM receivers using envelope detection. 5 a.
 - (10 Marks) Explain the noisy receiver model with neat diagram. Explain briefly the figure of merit. b.
 - (06 Marks) Explain the noise equivalent bandwidth with relevant equation. c. (04 Marks)

(10 Marks)

(06 Marks)

(09 Marks)

- Derive the expression for Figure Of Merit (FOM) for DSBSC receiver. 6 a.
 - b. Explain the use of pre-emphasis and de-emphasis circuit in an FM system. (06 Marks)
 - Define the white noise. Briefly explain the power spectral density and autocorrelation c. function of white noise. (04 Marks)

Module-4

- State sampling theorem. Write the mathematical form of sampled signal and explain the 7 a. steps to reconstruct the signal g(t) from the sequence of sample value. (10 Marks)
 - Explain the concept of TDM with a neat block diagram. b.
 - What is aperture effect? Briefly explain how to overcome this effect. C. (04 Marks)

OR

8 Briefly explain the following pulse modulation with waveform: a. iii) PPM. i) PAM ii) PWM

With neat block diagram, explain the generation of PPM wave. b. (05 Marks)

- Explain the following terms: C.
 - Under sampling i)
 - Over sampling ii)
 - Nyquist rate. iii)

(06 Marks)

Module-5

- Derive the expression of output signal to noise ratio of a uniform quantizer. 9 a. (08 Marks) With neat block diagram, explain the transmitter, transmission path and receiver of a PCM b.
 - system. (08 Marks)
 - An audio signal digitalized using PCM. Assume the audio signal bandwidth to be 20kHz. C.
 - What is the Nyquist rate and Nyquist period of the audio signal? i)
 - If the samples are quantized to L = 4096 levels and then binary coded, determine the ii) (04 Marks) number of bits required to encode a sample.

OR

- Draw the line codes for given binary representation 01101001 10 a.
 - i) Unipolar NRZ signaling
 - ii) Polar NRZ signaling
 - Unipolar RZ signaling iii)
 - iv) Bipolar RZ signaling
 - v) Manchester code.

b. Explain granular noise and slope overload distortion in delta modulation.

c. With neat diagram explain delta modulation system.

(10 Marks) (04 Marks)

(06 Marks)

18EC54

Fifth Semester B.E. Degree Examination, Feb./Mar.2022 **Information Theory and Coding**

GBGS SGHEME

Time: 3 hrs.

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Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- Define self information. Why logarithmic expression is chosen for measuring information. 1 a. (04 Marks)
 - (i) Find relationship between Hartleys, nats and bits. b.
 - (ii) A discrete source emits one of the four symbols S_0 , S_1 , S_2 and S_3 with probabilities 1/3, 1/6, 1/4 and 1/4 respectively. The successive symbols emitted by the source are statistically independent. Calculate the entropy of the source. (08 Marks)
 - (i) State the properties of entropy. c.

(i)

(ii) A source transmits two independent messages with probabilities of P and 1-P respectively. Prove that the entropy is maximum when both the message are equally likely. Plot the variation of entropy (H) as a function of probability 'P' of the messages.

(iv) G_1, G_2

(08 Marks)

(10 Marks)

OR

- Consider the following Markov source shown in Fig. Q2 (a). Find the 2 a.
 - State probabilities (ii) State entropies.
 - (iii) Source entropy.
 - Show that $G_1 > G_2 > H$ (v)

A2/3 Fig. Q2 (a)

- b. Consider a zero memory source emitting three symbols x, y and z with respective probabilities {0.6, 0.3, 0.1}. Calculate
 - (i) Entropy of the source.

- (ii) All symbols and the corresponding probabilities of the second order extension of the source. Find the entropy of the second-order extension of the source.
- (iii) Show that $H(s^2) = 2 * H(s)$

Module-2

3 The table 3.1 below provides codes for five different symbols. Identify which of the a. following codes are prefix codes. Also draw the decision diagram for the prefix codes.

(04 Marks)

(10 Marks)

, y					
Code A	Code B	Code C	Code D		
0	1	00	10		
10	01	110	111		
110	111	1110	110		
1110	1110 10		01		
111	00	011	00		

(10 Marks)

b. Apply Shannon's encoding algorithm to the following set of messages and obtain code efficiency and redundancy. (10 Marks)

m_1	m ₂	m3	m4	m ₅
1	1	3	1	3
8	16	16	4	8

c. Construct a Binary code by applying Huffman encoding procedure for the following messages with respective probabilities of 0.4, 0.2, 0.2, 0.1, 0.07 and 0.03. Also determine the code efficiency and redundancy of the code. (06 Marks)

OR

Design a Trinary source code for the source shown using Huffman's coding procedure: a. $S = \{S_1, S_2, S_2, S_4, S_5, S_6\}$

$$\mathbf{P} = \left\{ \frac{1}{3}, \frac{1}{4}, \frac{1}{8}, \frac{1}{8}, \frac{1}{12}, \frac{1}{12} \right\}$$

4

b. Consider a source $S = \{S_1, S_2\}$ with probabilities $\frac{3}{4}$ and $\frac{1}{4}$ respectively. Obtain Shannon-Fano code for source S, its 2nd and 3rd extension. Calculate efficiencies for each case and justify the results. (10 Marks)

Module-3

5 What is mutual information? Mention its properties. (06 Marks) a. A transmitter has an alphabet consisting of 5 letters $\{a_1, a_2, a_3, a_4, a_5\}$ and the receiver has an b. alphabet of four letters $\{b_1, b_2, b_3, b_4\}$. The joint probabilities of the system are given below:

 b_1 b_2 b₃ b₄ P(A, B) =0.25 a_1 0 0 0.10 0.30 0 0 a_2 0.05 0.10 0 0 az 0 0.05 0.1 a_4 0 0.05 0 a_5

Compute different entropies of the channel.

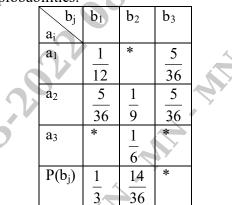
For the channel matrix shown, find the channel capacity. c.

> b_1 b_2 b_3 $\frac{1}{6}$ $\frac{1}{2}$ 1 $\frac{\overline{2}}{1}$ $\frac{1}{3}$ $\overline{\frac{1}{3}}$ $\frac{1}{6}$ 1a₂ 2 3

(06 Marks)

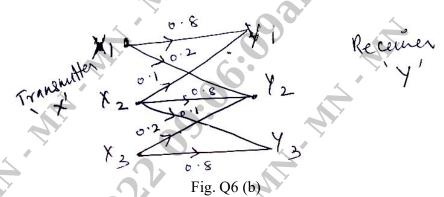
(08 Marks)

6 a. In a communication system a transmitter has 3 input symbols $A = \{a_1, a_2, a_3\}$ and receiver also has 3 output symbols $B = \{b_1, b_2, b_3\}$. The matrix given below shows joint probability matrix with some marginal probabilities. (06 Marks)



- (i) Find the missing probabilities (*) in the table.
- (ii) Find $P(b_3/a_1)$ and $P(a_1/b_3)$
- (iii) Are the events a_1 and b_1 statistically independent? Why?
- b. Find the capacity of the channel shown in the Fig. Q6 (b) below using Murugo's method.

(08 Marks)



c. Discuss Binary Ensure channel and derive channel capacity equation.

(06 Marks)

Module-4

- 7 a. For a systematic (7, 4) linear block code, the parity matrix P is given by,
 - $\begin{bmatrix} P \end{bmatrix} = \begin{vmatrix} 1 & 1 & 0 \\ 1 & 0 & 1 \\ 0 & 1 & 1 \end{vmatrix}$
 - (i) Find all possible code vectors.
 - (ii) Draw the encoding circuit.
 - (iii) Draw the syndrome calculation circuit. (10 Marks)
 - b. Design an encoder for a (7, 4) binary cyclic code generated by $g(x) = 1 + x + x^3$ and verify its operation using the message vectors (1 0 0 1) and (1 0 1 1). (10 Marks)

4 of 4

18EC54

- 8 a. Define G and H matrix and show that $GH^T = 0$.
 - b. The Parity check bits of a (8, 4) block code are generated by,
 - $C_5 = d_1 + d_2 + d_4$
 - $\mathbf{C}_6 = \mathbf{d}_1 + \mathbf{d}_2 + \mathbf{d}_3$
 - $\mathbf{C}_7 = \mathbf{d}_1 + \mathbf{d}_3 + \mathbf{d}_4$

 $C_8 = d_2 + d_3 + d_4$

where d_1 , d_2 , d_3 , d_4 are the message bits.

- (i) Find the generator and parity matrix for this code.
- (ii) Find the minimum weight.
- (iii) Show that its capable of correcting all single error pattern and capable of detecting double errors by preparing the syndrome table for them. (10 Marks)
- c. Design a linear block code with minimum distance $d_{min} = 3$ and message length of 4 bits.

(05 Marks)

<u>Module-5</u>

9 a. With a neat block diagram, draw a general decoding circuit for a linear block code. Also draw the complete error correcting circuit for a (7, 4) linear block code if the error bits are given in terms of the syndrome bits as given in equation below:

 $\mathbf{S} = \begin{bmatrix} \mathbf{S}_1 \ \mathbf{S}_2 \ \mathbf{S}_3 \end{bmatrix} = \begin{bmatrix} (\mathbf{r}_1 + \mathbf{r}_2 + \mathbf{r}_3 + \mathbf{r}_5), (\mathbf{r}_1 + \mathbf{r}_2 + \mathbf{r}_4 + \mathbf{r}_6), (\mathbf{r}_1 + \mathbf{r}_3 + \mathbf{r}_4 + \mathbf{r}_7) \end{bmatrix}.$ (06 Marks)

- b. Consider a (7, 4) cyclic code with $g(x) = 1 + x + x^3$. Obtain the code polynomial in non systematic and systematic form for the input sequence.
 - (i) 1010
 - (ii) 1100
- c. Write short notes on BCH codes.

OR

- **10** a. For a (2, 1, 3) convolutional encoder with $g^{(1)} = 1 \ 0 \ 1 \ 1$ and $g^{(2)} = 1 \ 1 \ 1 \ 1$. Find the output sequence using the two following approaches:
 - (i) Time domain approach.
 - (ii) Transform domain approach.

Also draw the encoder diagram.

b. For a (2, 1, 2) convolutional encoder with $g^{(1)} = [1 \ 1 \ 1], g^{(2)} = [1 \ 0 \ 1]$

- (i) Draw the transition table.
- (ii) State diagram.
- (iii) Draw code tree.
- (iv) Using the code tree, find the encoded sequence for the message 1 0 1 1 1.
- (v) Draw the Trellis diagram.

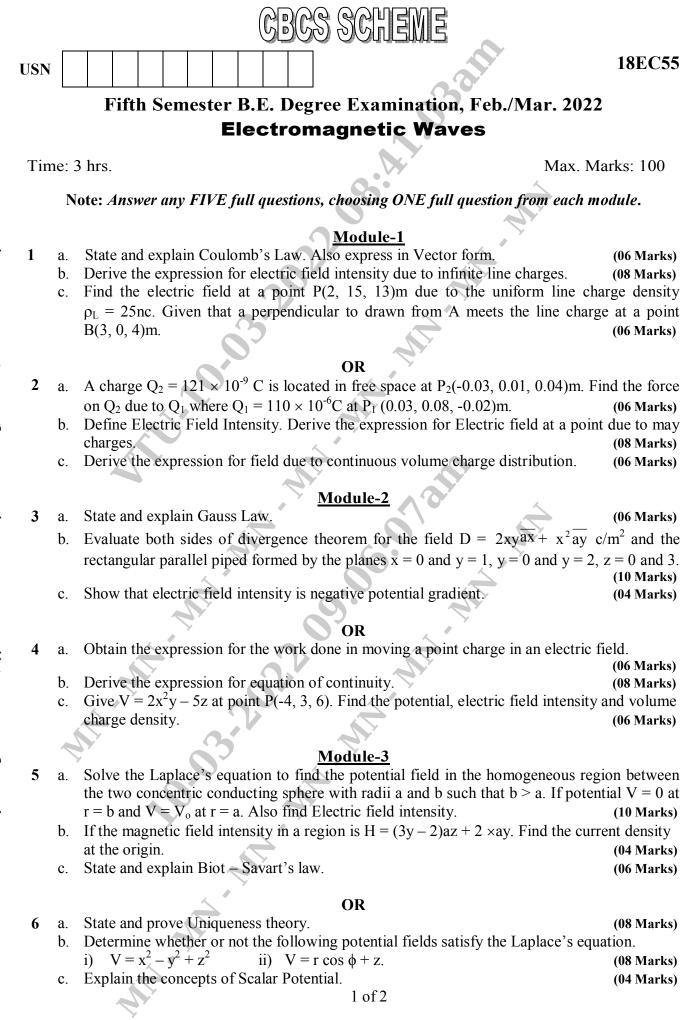
(05 Marks)

(10 Marks)

(10 Marks)

(10 Marks)

(04 Marks)



Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8=50, will be treated as malpractice. Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.

Module-4

- Derive an expression for force between differential current elements. 7 a. (06 Marks)
 - b. Obtain the boundary conditions at the interface between two magnetic materials. (10 Marks) c. Find the magnetization in a magnetic material, where
 - i) $\mu = 1.8 \times 10^{-5}$ H/m and H = 120 A/m ii) $B = 300\mu T$ and suspectibility = 15. (04 Marks)

- State and explain Faraday's law of Electromagnetic Induction. Show its equation in 8 a. differential form and integral form. (10 Marks)
 - b. A point charge Q = 18nc has a velocity of 5×106 m/s in the direction $a_v = 0.6 \overline{a_x} + 0.75 \overline{a_y} + 0.3 \overline{a_z}$. Calculate the magnitude of force exerted on the charge by the field i) $\overline{E} = -3\overline{a_x} + 4\overline{a_y} + 6\overline{a_z}$ Kv/m ii) $\overline{B} = -3a_x + 4\overline{a_y} + 6\overline{a_z}$ MT iii) \overline{B} and \overline{E} acting together.
 - A conductor of length 4m long lies along the Y axis with a current of 10 Amp in the a_y C. direction. Find the force on the conductor if the field in the region is $B = 0.005 \overline{a_x}$ tesla. (04 Marks)

Module-5

- What is meant by Uniform Plane Wave? Derive the expression for Uniform Plane Wave in 9 a. the free space. (10 Marks)
 - Let $\mu = 10^{-5}$ H/m, $\epsilon = 4 \times 10^{-9}$ F/m, $\sigma = 0$ and $\rho_v = 0$. Determine 'K' so that each of the b. following pair of fields satisfies Maxwell's equation :

i)
$$\vec{D} = 2x \hat{a}_x - 3y \hat{a}_y + 4z \hat{a}_z nC/m^2$$
, $\vec{H} = Kx \hat{a}_x + 10y \hat{a}_y - 25z \hat{a}_z A/m$

ii)
$$\vec{E} = (20y - kt)\hat{a}_x V/m$$
, $\vec{H} = (y + 2 \times 10^6 t)\hat{a}_z A/m$. (10 Marks)

OR

- State and explain Poynting's theorem. 10 a.
 - b. Discuss Wave propagation in good conducting medium. (06 Marks)
 - c. Find the frequency at which conduction current density and displacement current density are equal in a medium with $\sigma = 2 \times 10^{-4}$ O/m and $\varepsilon_r = 81$. (04 Marks)

(06 Marks)

(10 Marks)

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		F	Fiftl	n Se	eme	ster	B.F	E. I)eg	ree Examination, Feb./Mar. 202	2
										erilog HDL	
Tim	ne: 3	3 hrs.								Max.	Marks: 100
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1	0	Evn	lain	o true	ical	locia	flor	v fo	r da	<u>Module-1</u> signing VLSI IC circuits using the block dia	CT 0 120
1	a.	Елр		atyp	ncart	lesigi	1 110	w 10		signing vLSi ic circuits using the block that	(10 Marks)
	b.	-			-	tance			s.		(05 Marks)
	c.	Exp	lain	the t	rends	in H	DLs.				(05 Marks)
						6				OR	
2	a.									action used for programming in verilog.	(08 Marks)
	b.	Writ	te the	e vei	ilog (code f	for 4	-bit	ripp	ble carry counter. Also write the stimulus.	(12 Marks)
										Module-2	
3	a.	-		× · · · · · · · · · · · · · · · · · · ·	-				<u> </u>	module with block diagram.	(06 Marks)
	b.	-				-				th an example in verilog.	
	c.	,	-		· ·	•	,			ters iv) Nets v) Integers.	(10 Marks) (04 Marks)
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4	a. b.									latch. Also write stimulus code. and \$stop system tasks with examples.	(10 Marks) (10 Marks)
	υ.	цир	lam	puis	jiay,		1101,	ψIII	11511	and stop system tasks with examples.	(10 Marks)
										Module-3	
5	a. h									ys? How they are specified in verilog?	(06 Marks)
	b.			N Y		-				lowing for $A = 4'b0111$ an $dB = 4'b1001$. $\{B\}\}$ v) $A^{A}B$ vi) $A B$ vii) $A*B$ viii) $A < = B$	(08 Marks)
	c.	,								an example for BUFIF1 and BUFIF0 primi	
		Δ					N				(06 Marks)
						0				OB	
6	a.	Desi	ign A	AOI	based	4 to	1 mu	ıltip	lexe	er and write the verilog description and its st	imulus.
	b.	Writ	te th		ilog (lata f	low (desc	rint	ion for 4-bit full adder with carry look –ahea	(10 Marks)
	υ.	**11			nog	aata 1		uese	, ipi	ion for 4 of full adder with early look and	(10 Marks)
					*			~		NT - J-1- 4	
7	a.	Exn	lain	bloc	kinos	and n	on-h	lock	ino	<u>Module-4</u> assignments with an example.	(10 Marks)
	b.	-			•				-	ration with a period of 20 units using forever	
	C	W7'	نہ <u>۱</u> .	. 4:4	f					-	(05 Marks)
	c.	w rit	le th	e a11	ieren	ces be	etwee	en ti	ie ta	asks and functions.	(05 Marks)
										OR	

CBCS SCHEME

8 a. Discuss sequential and parallel blocks with examples.
b. Write a verilog program for 8 : 1 multiplexer using case statement.
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Module-5

- Write the verilog description for \overline{D} flipflop using assign and deassign procedural 9 a. continuous assignments. (10 Marks) (10 Marks)
 - b. Explain defparam statement with an example.

OR

What is logic synthesis? Explain the flow diagram for the designer's mind as the logic 10 a. synthesis tool. (10 Marks)

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b. What will be the following statements translate to when run on a logic synthesis tool : Assign {C-out, sum } = a + b + C in ; Assign out = (s)? i1 : i0, (10 Marks)

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(16 Marks)

(04 Marks)

Seventh Semester B.E. Degree Examination, Feb./Mar. 2022 Computer Networks

CBCS SCHEME

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

<u>Module-1</u>

a. Describe significant services of all layers in TCP/IP protocol suite along with the encapsulation and decapsulation processes with necessary figures.
b. List different performance criteria of a network.
(04 Marks)

OR

- **2** a. Explain different physical structures and networks topologies with the help of diagrams.
 - b. Distinguish TCP/IP model with OSI model.

Module-2

- Describe various fields in the format of an ARP packet and explain how ARP sends request 3 а and response messages. (12 Marks) Write short notes on implementation of standard Ethernet topologies. b. (08 Marks) ÓR Describe the concept of bit stuffing and byte stuffing. 4 a. (10 Marks) Explain CSMA/CD working with the help of flowchart b. (06 Marks) List the characteristics of wireless LANs. c. (04 Marks) **Module-3** Explain working of DHCP [Dynamic Host Configuration Protocol]. 5 (08 Marks) a. b. Inspect the following MAC addresses and categories them as unicast, multicast and broadcast. 4A:30:10:21:10:1A i) 47:20:1B:2E:08:EE ii) iii) EF : FF : 10 : 01 : 11 : 00 iv) FF : <u>FF</u> : FF : FF : FF (04 Marks) Explain IPV4 datagram format with a neat diagram. c. (08 Marks) OR Explain a simple implementation of Networks Address Translation (NAT). 6 (10 Marks) a. Explain distance vector routing algorithm using Bellman ford equations. b. (10 Marks) Module-4 Describe connectionless and connection - oriented services provided by the transport layer. 7 a. (14 Marks) Describe the general services provided by UDP. (06 Marks) b. OR Explain working of Go-back-N protocol. 8 (10 Marks) a. Describe sending and receiving buffers in TCP, and explain how segments are created form b. the bytes in the buffers. (10 Marks) Module-5
- 9 a. Explain the architecture and format of electronic mail.(10 Marks)b. Distinguish Local Logging and Remote Logging.(10 Marks)

OR

10a. Explain persistent and non-persistent connections in HTTP.(10 Marks)b. Write a short note on DNS recursive and iterative resolutions.(10 Marks)

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Seventh Semester B.E. Degree Examination, Feb./Mar. 2022 VLSI Design

CBCS SCHEME

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- With necessary circuit diagram, explain the operation of tristate inverter. Also realize a 2 : 1 a. multiplexer using tristate inverter. (08 Marks)
 - Implement a D flipflop using transmission gates and explain its operation with necessary b. tining diagram. (08 Marks)
 - Realize CMOS compound gate for the function Y = A(B+C) + DE. (04 Marks) c.

OR

- Explain the operation of MOSFET with necessary diagrams. Also derive the equation for a. drain current in linear and saturation region of operation. (10 Marks)
 - Draw the circuit of CMOS inverter and explain its DC transfer characteristics. (06 Marks) b.
 - Explain the following non-ideal effects channel length modulation, mobility degradation. c.

(04 Marks)

Module-2

Explain CMOS n-well fabrication process with necessary diagrams. 3 (12 Marks) a. What is scaling. Compute drain current, power, current density and power density for b. constant field and constant voltage scaling. (08 Marks)

OR

- a. Draw the layout of Y = (A + B + C)D and estimate the area. (08 Marks) Mention different types of MOSFET capacitances and explain with necessary diagrams and b. equations. (06 Marks) c. With neat diagram, explain lambda based design rules for wires and contacts. (06 Marks)

Module-3

- Develop the RC delay model to compute the delay of the logic circuit and calculate the delay a. of unit sized inverter driving another unit inverter. (08 Marks)
 - b. Explain Cascode Voltage Switch Logic (CVSL). Also realize two input AND/NAND using CVSL. (06 Marks)
 - c. Explain linear delay model. Compare the logical efforts of the following gates with the help of schematic diagrams :
 - i) 2-input NAND gate ii) 3-input NOR gate.

(06Marks)

OR

- Explain : i) pseudo nMOS ii) ganged CMOS with necessary circuit examples. 6 (06 Marks) a. Estimate t_{pdf} and t_{pdr} of a 3-input NAND gate if the output is loaded with h identical gates. b.
 - Use Elmore delay model. (08 Marks) (06 Marks)
 - Explain skewed gates with an example. c.

(08 Marks)

Module-4

- 7 With necessary circuit diagrams, explain resettable latches with a. i) synchronous reset ii) asynchronous reset.
 - b. Compute the output voltage V_{out} in the following pass transistor circuits. Assume $V_t = 0.7$. (Ref. Fig.Q7(b)).

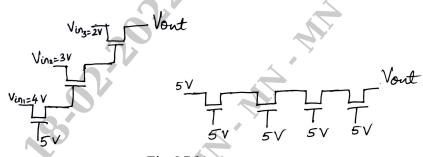


Fig.Q7(b)

(06 Marks)

(08 Marks)

c. With necessary diagram, explain a D flipflop with two-phase non-overlapping clocks. (06 Marks)

OR

- With necessary circuit diagram explain 3-bit dynamic shift register with depletion load. 8 a.
 - Realize $F = \overline{A_1A_2A_3 + B_1B_2}$ using dynamic CMOS logic. Also explain the cascading b. problem in dynamic logic with necessary example. (08 Marks)
 - c. Explain the general structure of ratioless synchronous dynamic logic with relevant diagram. (04 Marks)

Module-5

- With necessary circuit diagram, explain the operation of three transistor DRAM cell. 9 a.
 - (08 Marks) Explain full CMOS SRAM cell with necessary circuit topology. b. (08 Marks)
 - Explain the terms : c.
 - i) Observability
 - ii) Controllability
 - iii) Fault coverage.

(04 Marks)

OR

What is a fault model? Explain stuck-at model with examples. 10 a. (07 Marks) Mention the approaches used in design for testability. Explain scan based testing using b.

- necessary diagrams. (07 Marks) (06 Marks)
- Draw the circuit of 3-bit BIST register and explain. c.

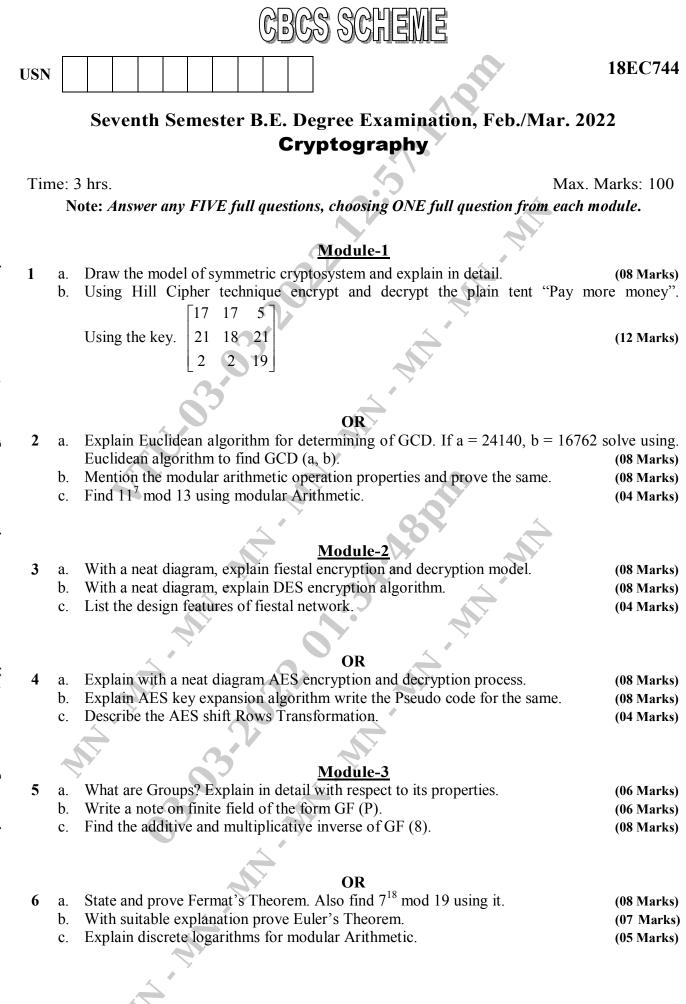
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Seventh Semester B.E. Degree Examination, Feb./Mar. 2022						
Real Time Systems						
Tir	ne: 🤅	3 hrs. Max. M	arks: 100			
Note: Answer any FIVE full questions, choosing ONE full question from each module.						
Module-1						
1	a.	Define real time system. Classify them based on time constraints.	(06 Marks)			
	b.	Write a short note on hierarchical system.	(04 Marks)			
	c.	Explain the different types of program in system design.	(10 Marks)			
		OR				
2	a.	Explain briefly sequence control with neat diagram.	(06 Marks)			
	b. с.	What is DDC? Explain with block diagram. Explain ISO seven layer model for data communication.	(06 Marks) (08 Marks)			
	С.					
3	0	Evaluin the different forms of norallel computer architectures	(12 Mardae)			
î J	a. b.	Explain the different forms of parallel computer architectures. Explain pulse interface for input and output operation with a neat block diagram.	(12 Marks) (08 Marks)			
			(00 10 10 10 10 10 10 10 10 10 10 10 10 1			
4	a.	OR Explain the basic interrupt input mechanism with diagram and flow chart.	(10 Marks)			
	b.	Explain local and wide area networks.	(10 Marks) (10 Marks)			
-		Madula 3				
5	a.	Explain the following :				
		i) Security ii) Readability iii) Portability iv) Efficiency.	(10 Marks)			
	b.	List out some major requirements that CUTLASS language has to meet.	(10 Marks)			
		OR				
6	a.	Write short notes on overview of real time languages.	(08 Marks)			
1 1	b.	What are the data types? Explain each one briefly.	(12 Marks)			
		Module-4				
7	a.	Explain with neat diagram structures of RTOS.	(10 Marks)			
	b.	Explain cyclic and preemptive scheduling strategies.	(10 Marks)			
ρ		OR				
8	a.	Draw and explain task state diagram.	(10 Marks)			
	b.	Explain the general structures of Input Output Subsystem (IOSS).	(10 Marks)			
		Module-5				
9	a.	With neat flow-chart describes single program approach with reference to RTS de	sign. (10 Marks)			
	b.	Explain software design of RTS using software module.	(10 Marks) (10 Marks)			
		OR				
10	a.	Explain the outline of abstract modeling approach of Ward and Mellor.	(12 Marks)			
10	b.	Write a short note on YOURDON METHODOLOGY.	(08 Marks)			

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Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. 2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

CBCS SCHEME



2. Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8=50, will be treated as malpractice. Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.

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Module-4

7	a.	With a neat diagram, explain public-key cryptosystem secrecy and Authenticatio	
	b. c.	Explain the steps involved for encryption and Decryption for RSA Algorithm. Perform encryption using RSA algorithm for $p = 5$, $q = 11$, $e = 3$, $m = 9$.	(06 Marks) (04 Marks)
	0.		
		OR	
8	a.	Explain Diffie-Hellman key exchange algorithm.	(07 Marks)
Ū	b.	Explain Elliptic curve over real numbers.	(07 Marks) (07 Marks)
	c.	Explain Elliptic curve cryptography.	(06 Marks)
		Module-5	
9	a.	Write an explanatory note on Liner Feedback shift registers.	(10 Marks)
	b.	Explain the following with necessary diagrams :	
		i) Generalized Geffe Generatorii) Threshold Generator	
		iii) Alternating stop and go generator.	(10 Marks)
		OR	
10	a.	Explain Additive Generators. Also explain fish and pike Additive Generator.	(10 Marks)
	b.	With a neat diagram, explain the concept of Gifford.	(06 Marks)
	c.	Write a short note on A5.	(04 Marks)

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